EC600K-CN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

Date: 2024-03-06

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-08-02	Reuben WANG/ Jeff SHEN	Creation of the document
1.0	2024-03-06	Reuben WANG/ Jeff SHEN	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC600K-CN module in QuecOpen® solution, including block diagrams of module design, power supply, USIM, UART, LCM, matrix keypad and audio interface.

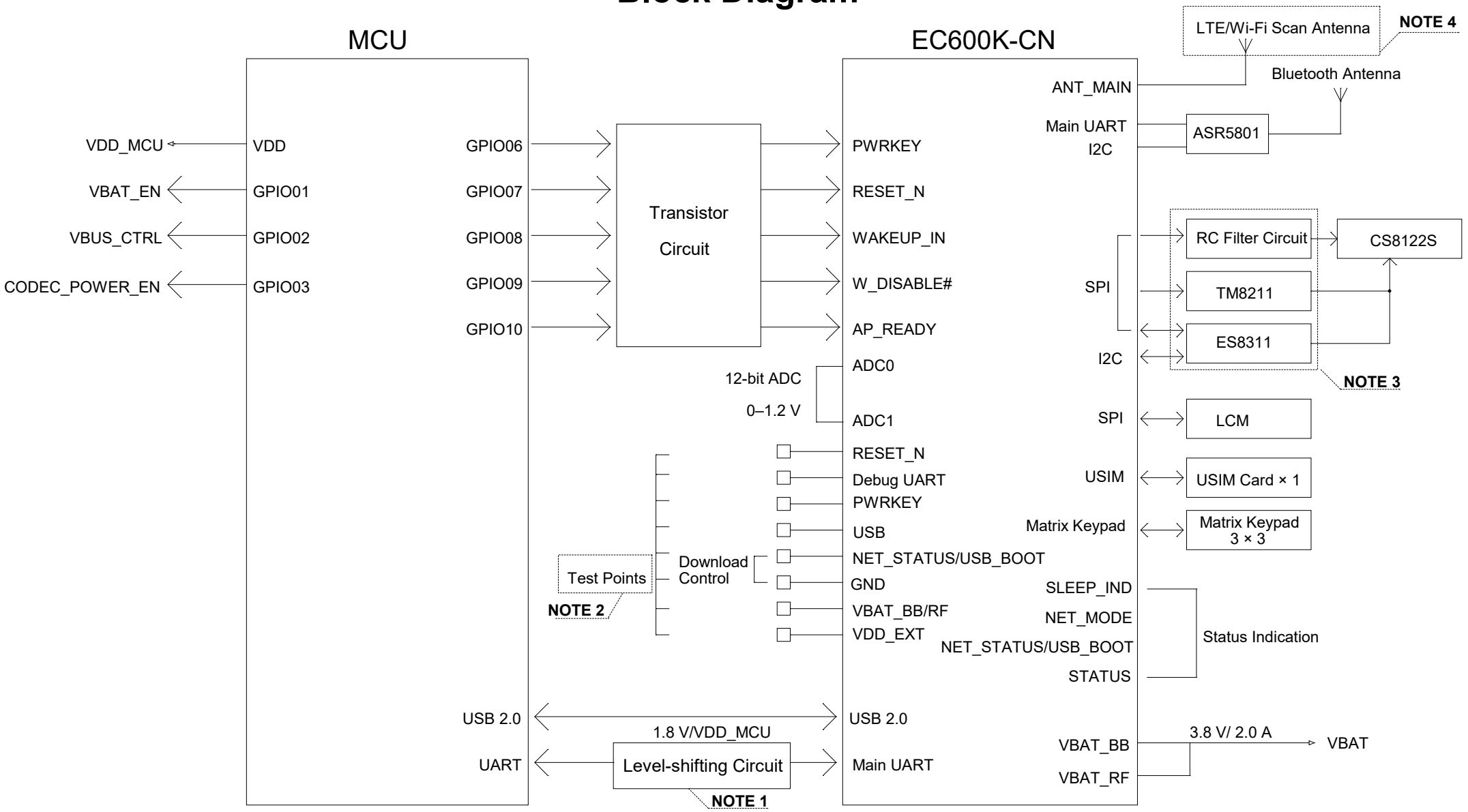
1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.
2. Test points must be reserved for DBG_TXD/RXD, USB_DP/DM and USB_VBUS. It is recommended to reserve test points for VDD_EXT, NET_STATUS/USB_BOOT, PWRKEY and VBAT_BB/RF. If RESET_N is unused, it is recommended to reserve a test point.
3. RC filter circuit design is used by default, and TM8211 or ES8311 circuit design can be selected externally for higher audio requirements.
4. Wi-Fi Scan function is optional, and the function shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.

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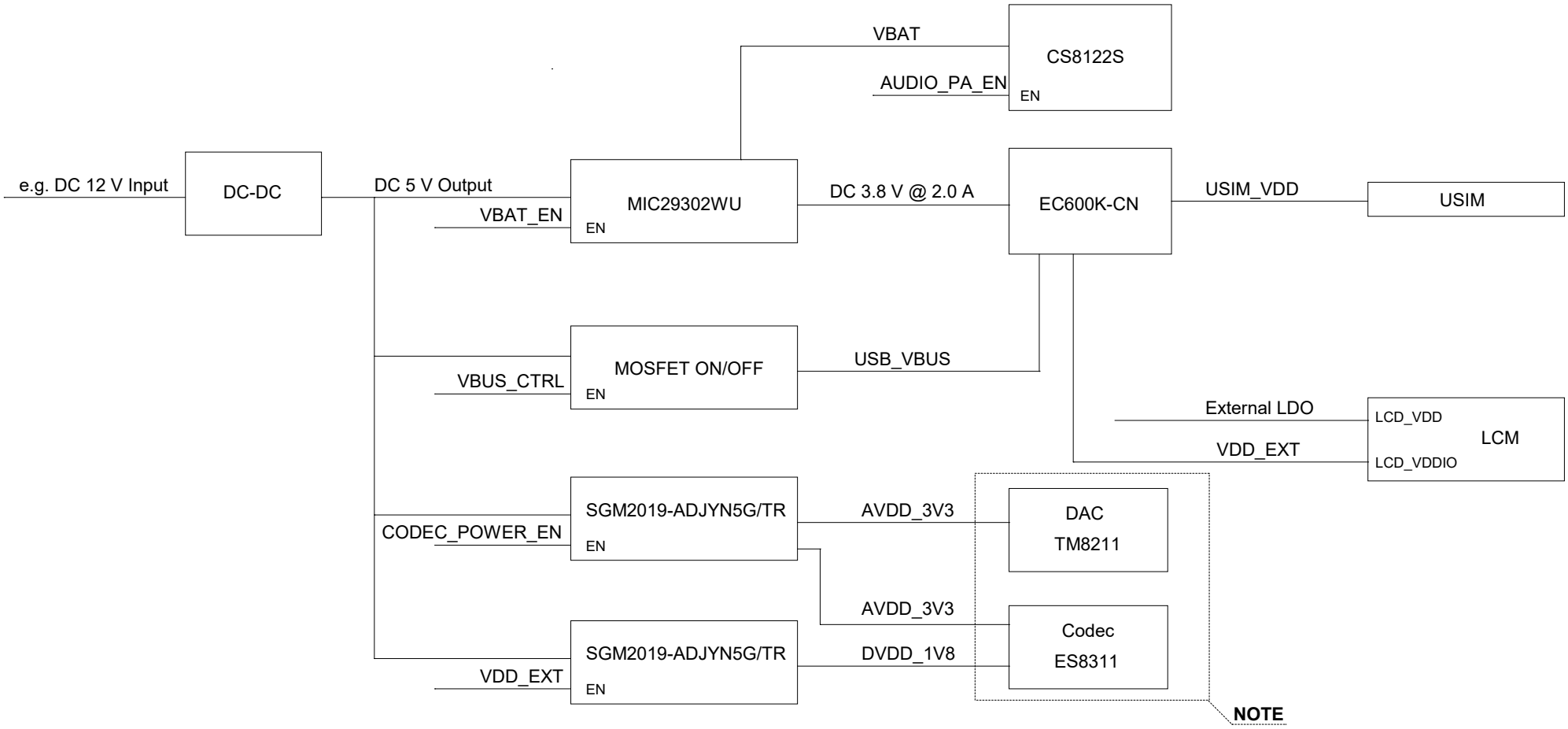
Power System Block Diagram



NOTE:

RC filter circuit design is used by default, and TM8211 or ES8311 circuit design can be selected externally for higher audio requirements.

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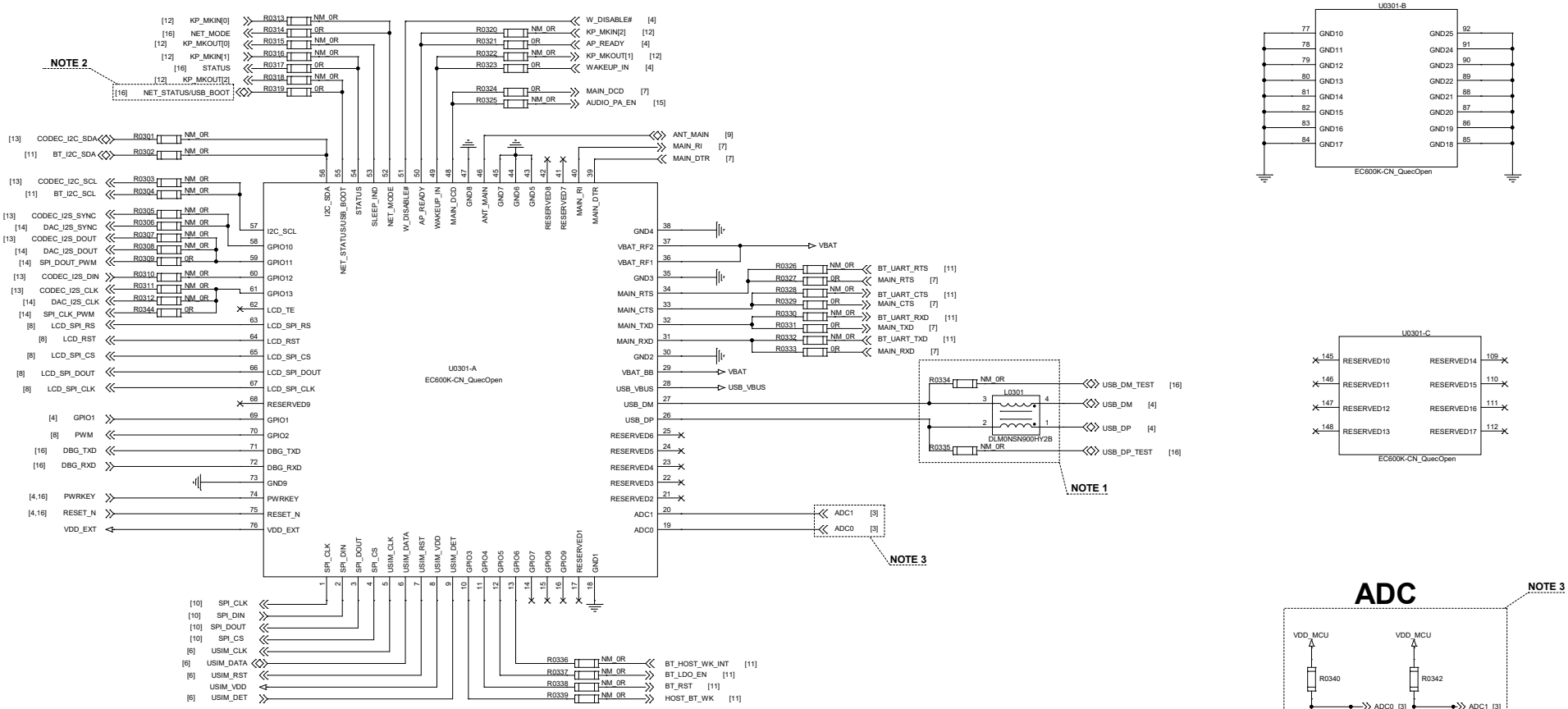
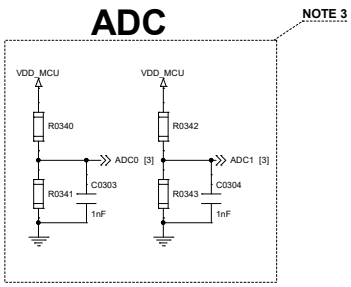
Module Interfaces



ADC



NOTE:

1. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI.
   Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.
   Place L0301 and two resistors R0334 and R0335 close to the module to ensure USB signal integrity.
2. NET_STATUS/USB_BOOT cannot be pulled down to low level before the module starts up successfully. Otherwise, the module will enter the forced download mode.
3. The voltage input range of ADC0 and ADC1 is 0–1.2 V. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 voltage inputs respectively, and the required resistance of the two resistors (R0340 and R0342) that connected to VDD_MCU is between 100 kΩ and 1 MΩ. The accuracy of the resistors directly affects ADC sampling error. It is recommended to use resistors with 1 % accuracy. For higher ADC accuracy, resistors with 0.5 % accuracy are recommended.
4. Connect all GND pins to ground, and keep unused and RESERVED pins open.
5. For more details of GPIO multiplexing function, see the GPIO configuration document of the module.
6. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer.
   At least four-layer board design is recommended.
7. The 6.0 and above version of QFlash tool must be used for firmware upgrading.

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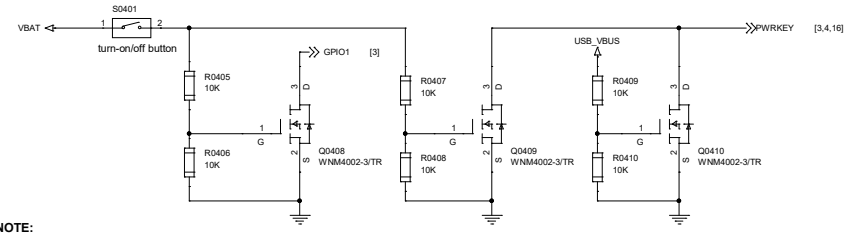
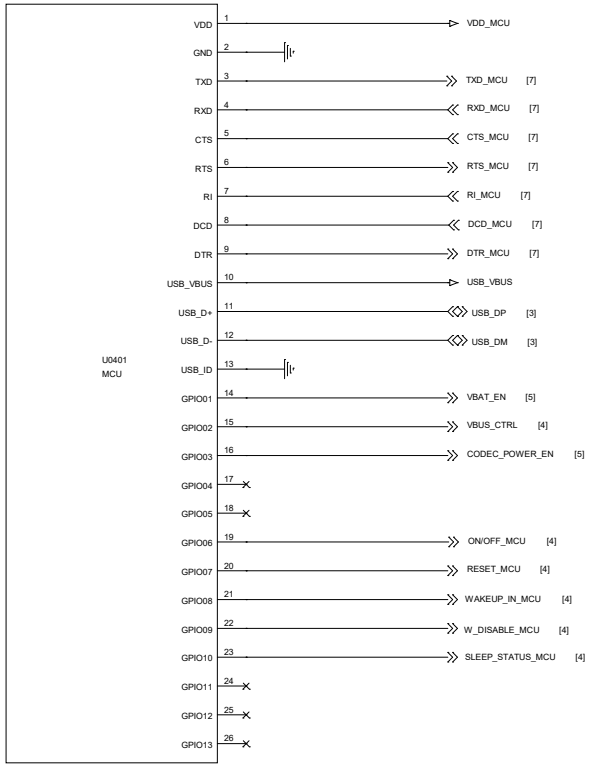
MCU Interfaces

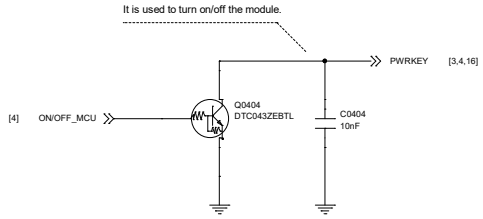
USB Insertion Enables Automatic Boot

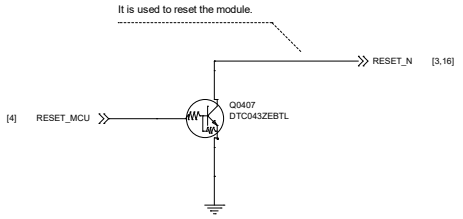


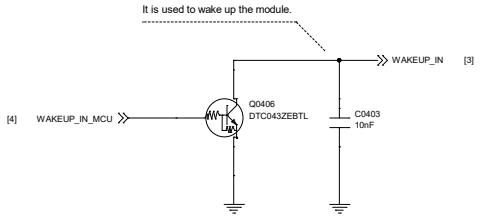
NOTE:

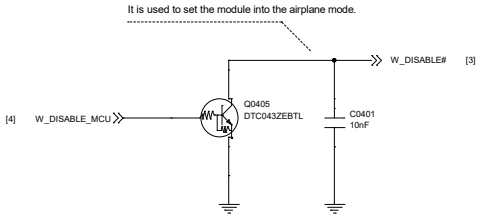
1. When USB is inserted, the module cannot be shut down normally, and will boot automatically after the shut down.
2. When USB is inserted, the level states of GPIO1 and PWRKEY pins are used to determine whether the module is turned on by the turn-on/off button or USB insertion. GPIO1 utilizes the GPIO resource with a default pull-up (PU) state.

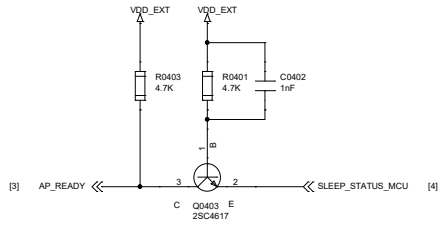


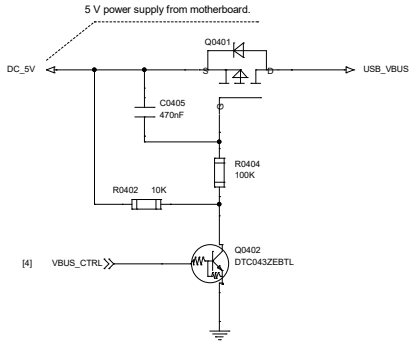












NOTE:

1. If the power domain of your MCU (U0401) is also 1.8 V, the level-shifting circuit is not necessary as it matches the 1.8 V power domain of the module's GPIO interfaces.
2. The USB interface of the module can only serve as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function. For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.

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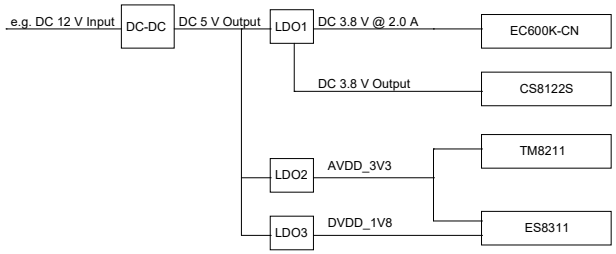
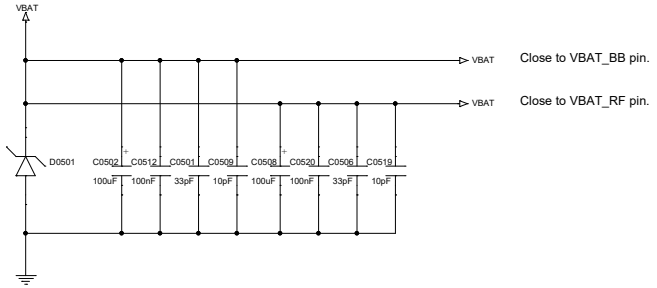
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, audio PA, DAC and Codec.



VBAT Design

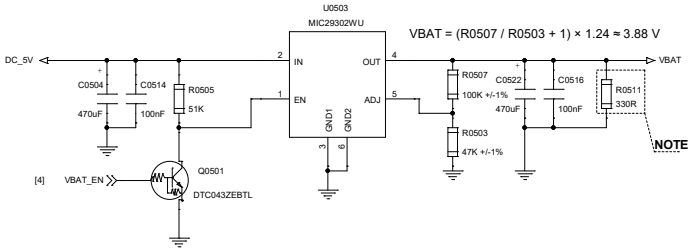


NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
2. The VBAT trace should be connected to VBAT_BB and VBAT_RF pins in a star configuration.
3. The width of VBAT_BB trace should be at least 1 mm; and the width of VBAT_RF trace should be at least 2 mm.
4. The recommended operating voltage range for VBAT is 3.4 V to 4.3 V, with a typical value of 3.8 V.

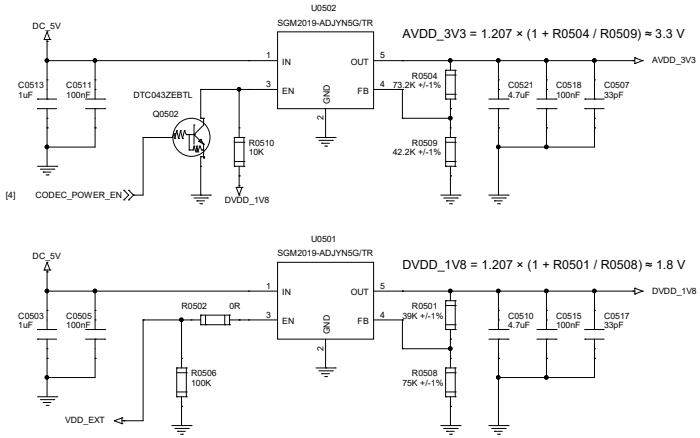
LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:
The recommended load current should exceed 10 mA.

Power Supply for Codec



NOTE:

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off DVDD_1V8 and AVDD_3V3 respectively.
2. To ensure proper functioning of the audio codec, adhere to the following power-up/down sequences:

   Power-up sequence: power on DVDD_1V8 first, followed by AVDD_3V3.

   Power-down sequence: power off AVDD_3V3 first, followed by DVDD_1V8.

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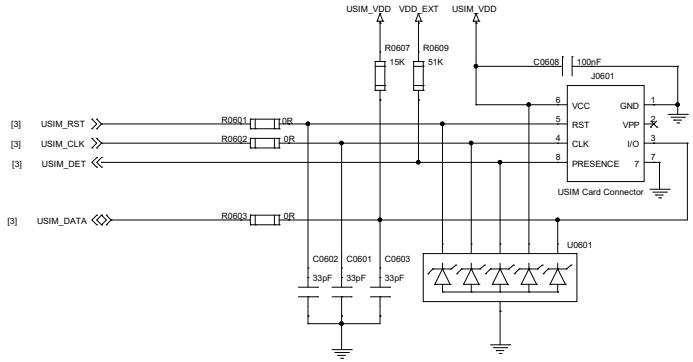
USIM Interface Design



NOTE:

1. It is recommended to use U0601 for effective ESD protection with a parasitic capacitance below 15 pF.
2. For USIM_DATA, it is recommended to add a 15 kΩ pull-up resistor R0607 near the USIM card connector to improve the anti-jamming capability of the USIM card.
3. R0601–R0603 are used for debugging, and C0601–C0603 are used for filtering out RF interference.
4. C0608's capacitance should be less than 1 μF and it should be placed close to the USIM card connector.

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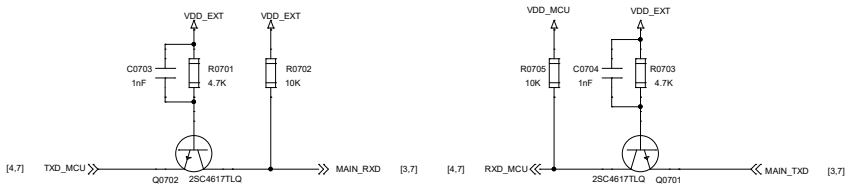
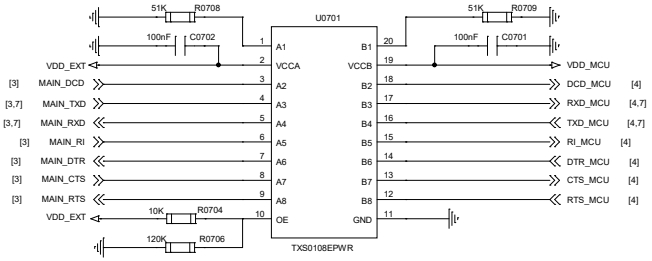
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0703 and C0704 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

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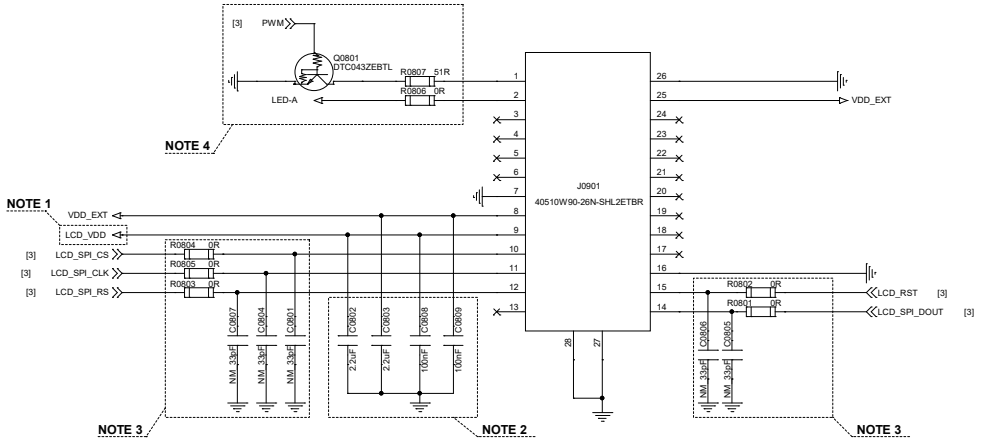
LCM Interface Design



NOTE:

1. It is recommended to design LCM power supply by yourself.
2. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.
3. Reserve 0 Ω resistors and 33 pF capacitors for the signal pins for debugging.
4. The LED-A backlight power supply should be designed by yourself. Select an appropriate resistor (R0807) based on the rated current of the digital transistor and the LED-A voltage value.

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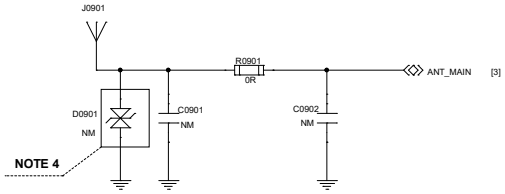
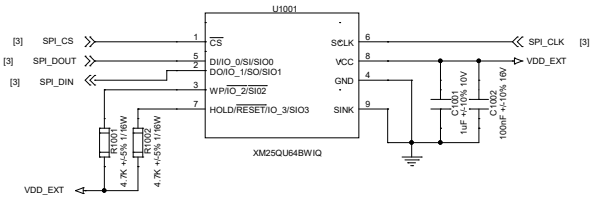
Antenna Interface Design



NOTE:

1. The single-ended impedance of the RF antenna is 50 Ω.
2. Reserve a Π-type matching circuit at antenna interface.
3. Wi-Fi Scan function is optional, and the function shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.
4. The junction capacitance of the antenna interface ESD protection component is recommended to be less than 0.05 pF.

SPI Design



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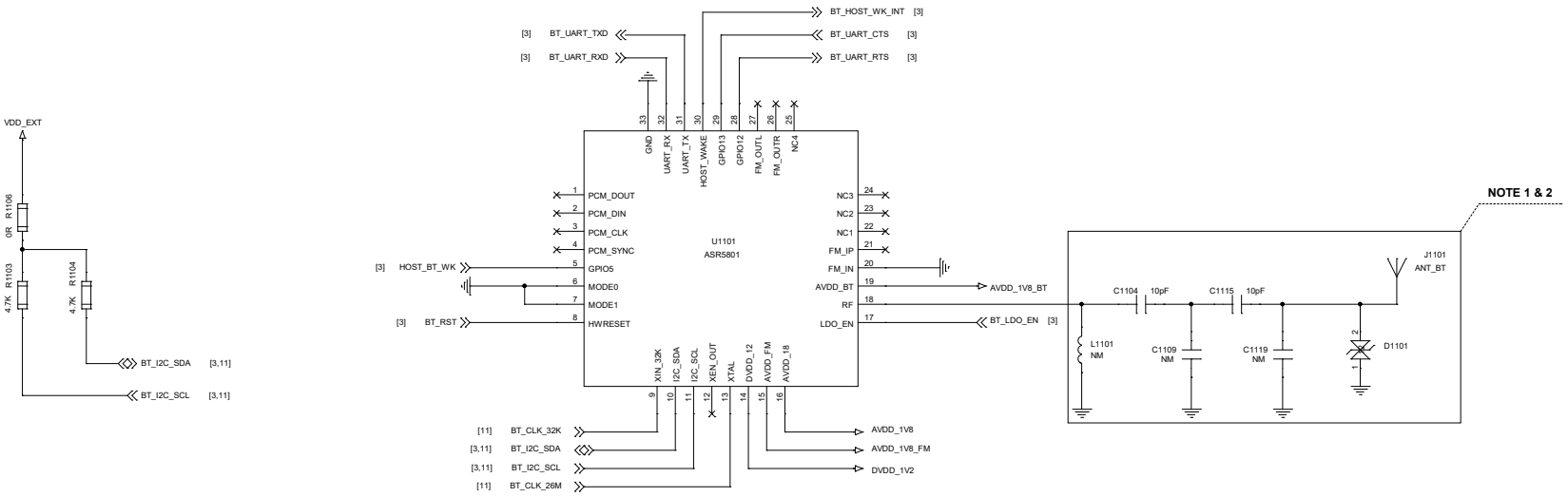
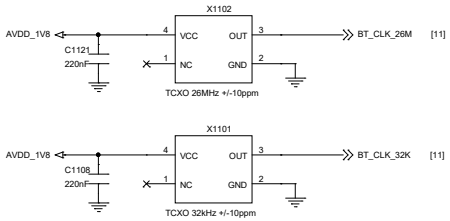
Bluetooth Interface Design



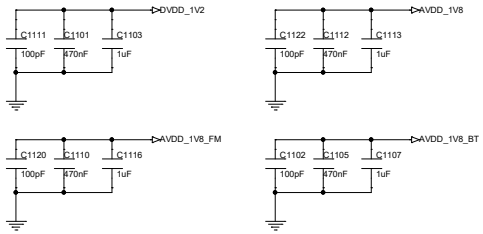
NOTE:

1. The single-ended impedance of the RF antenna is 50 Ω.
2. The junction capacitance of the antenna interface ESD protection component is recommended to be less than 0.05 pF.



NOTE:

26 MHz and 32 kHz oscillators are recommended to be used and you need to design power supply circuits on your own.



NOTE:

Design the 1.8 V power supply (AVDD_1V8) for the Bluetooth chip to provide the required voltage for its operation. The remaining three power supply pins (DVDD_1V2, AVDD_1V8_FM, and AVDD_1V8_BT) are internal power supply pins of the chip to be connected to external filter capacitors.

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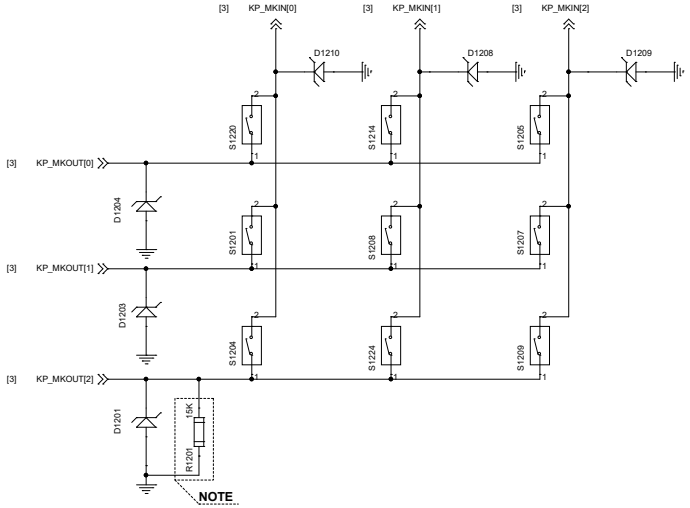
Matrix Keypad Interface Design



NOTE:
When pin 55 (NET_STATUS/USB_BOOT) of the module is multiplexed into KP_MKOUT[2], it must be pulled down to the ground by adding an external 15 kΩ resistor.

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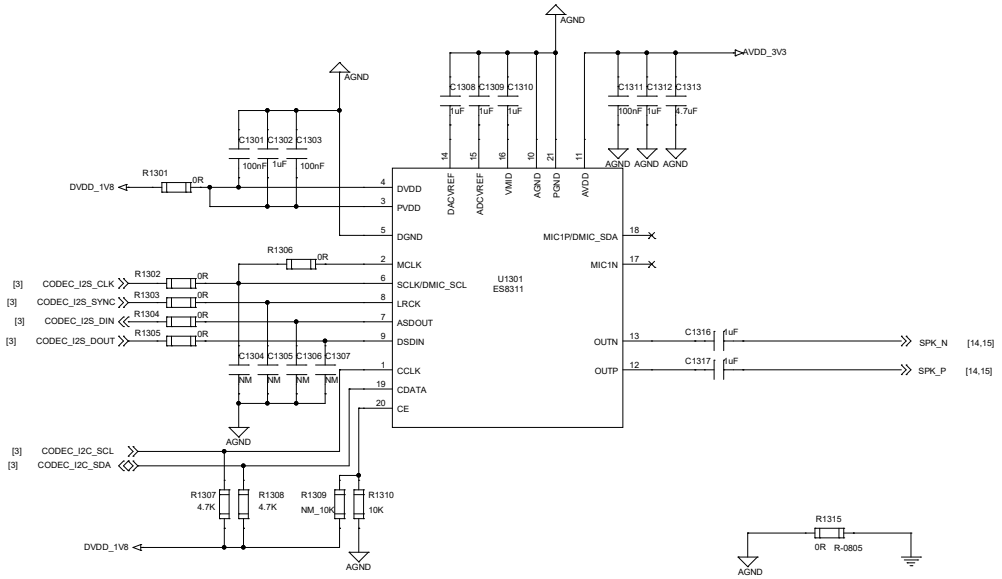
Audio Codec Design (ES8311)



NOTE:

1. When connected to the ES8311, the audio only supports downlink output, and does not support uplink input.
2. Differentiate between analog ground and digital ground. Analog ground should have a direct via to digital GND through a 0 Ω resistor (R-0805).

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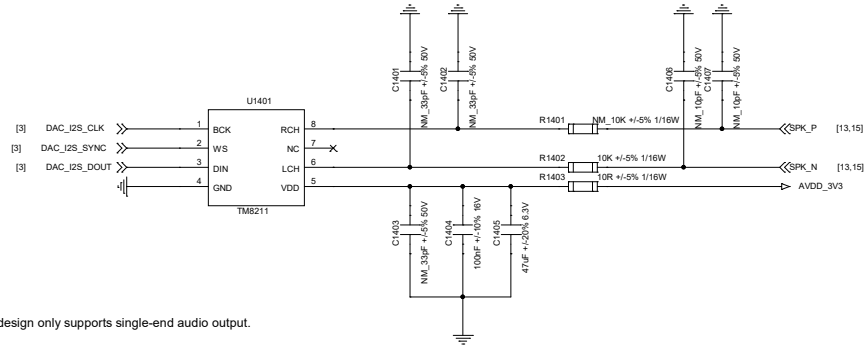
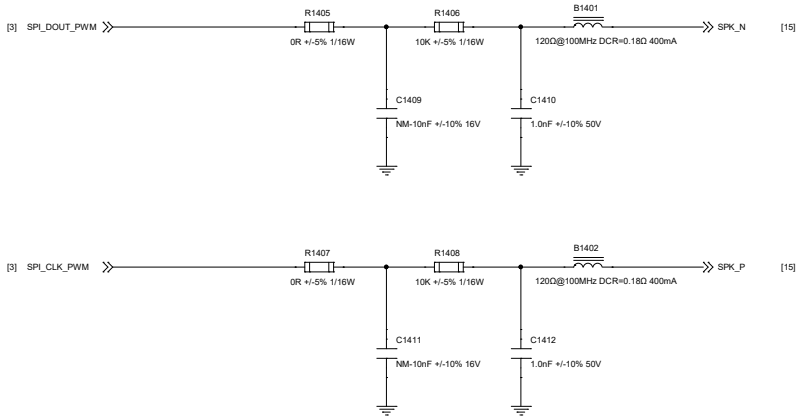
Audio Interface Design

TM8211 (DAC)



NOTE:
TM8211 circuit design only supports single-end audio output.

PWM (RC-Filter circuit)



NOTE:
RC filter circuit design is used by default, and TM8211 or ES8311 circuit design can be selected externally for higher audio requirements.

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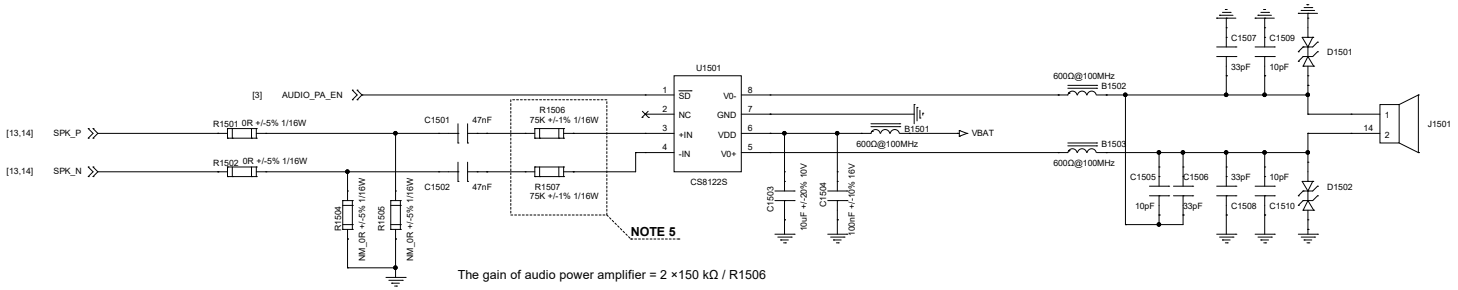
Analog Audio Design (Audio Power Amplifier)



The gain of audio power amplifier = 2 ×150 kΩ / R1506

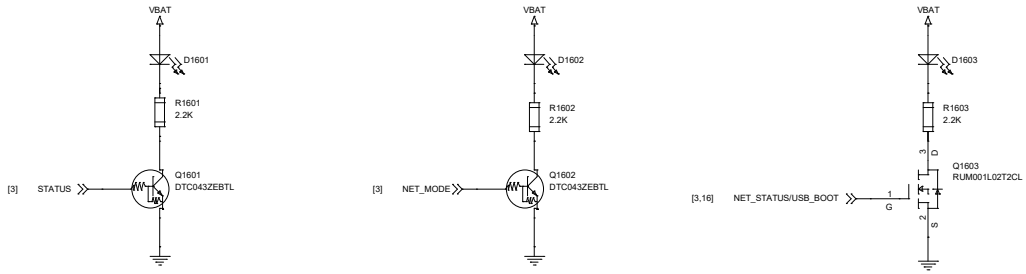
	ES8311	TM8211	PWM
R1501	0R	NM	0R
R1502	0R	0R	0R
R1504	NM	NM	NM
R1505	NM	0R	NM

NOTE:

1. SPK_P and SPK_N channels are differential output channels intended for connecting to an external audio power amplifier.
   To eliminate Pop noise, it is recommended to utilize MAIN_DCD of the module as the control signal for the audio power amplifier's enable pin.
   For more information about AUDIO_PA_EN, please contact Quectel Technical Support.
2. The type of power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to your actual needs.
3. When designing the layout, ensure that filter capacitors and ESD protection components are placed close to the loudspeaker to filter out interference and provide adequate protection.
4. The selection of ESD protection components should consider the output voltage range of the audio power amplifier. Ensure that the output voltage of the amplifier remains within the maximum reverse working voltage range of the selected ESD protection components under normal operating conditions.
   This precaution helps prevent damage to the ESD protection components.
5. R1506 and R1507 resistors are used to adjust the audio PA gain which is not recommended to exceed 10 times.

Other Designs

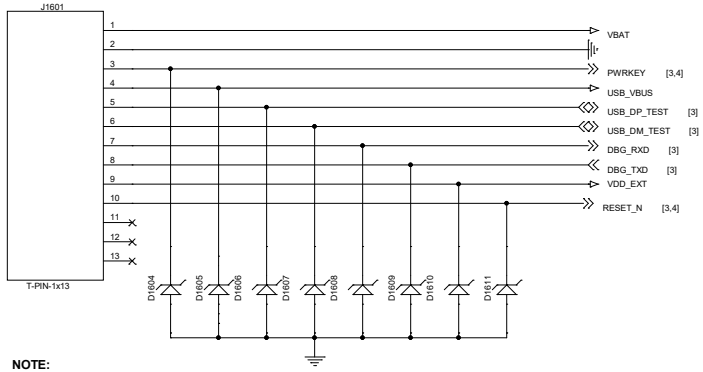
Indicators



NOTE:

1. For more details about STATUS, NET_MODE and NET_STATUS/USB_BOOT, see the hardware design document of the module.
2. To minimize the module's power consumption during the sleep mode of your device, replace the power supply (VBAT) of the STATUS, NET_MODE and NET_STATUS/USB_BOOT indicators with externally controllable sources and turn off the indicators when the module is in sleep mode.
3. Note that the maximum value of the MOSFET Q1603's Vgs (th) should not exceed 1 V, since the NET_STATUS/USB_BOOT pin of the module outputs high level by default. If a transistor such as Q1601 and Q1602 is used to replace the MOSFET, the NET_STATUS/USB_BOOT pin will be pulled down to low-level, and the module will enter the forced download mode and cannot be turned on normally.

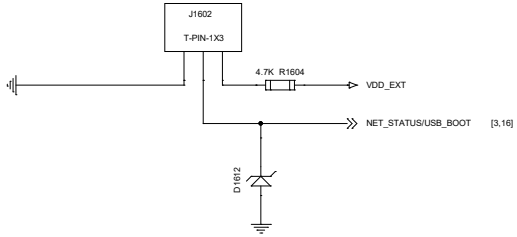
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrading.
3. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
4. The debug UART interface supports a 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.

USB_BOOT Interface



NOTE:

1. Make sure to reserve the USB_BOOT interface design and it is recommended to reserve a test point for this pin.
2. Before turning on the module, pull NET_STATUS/USB_BOOT down to GND to activate the forced download mode. This mode enables firmware upgrades via the USB interface.
3. The 6.0.1 and above version of QFlash tool must be used for firmware upgrading.

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