EC600E-CN QuecOpen Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-03-07	Fanny CHEN	Creation of the document
1.0	2023-07-14	Fanny CHEN	First official release

Contents

1 Reference Design

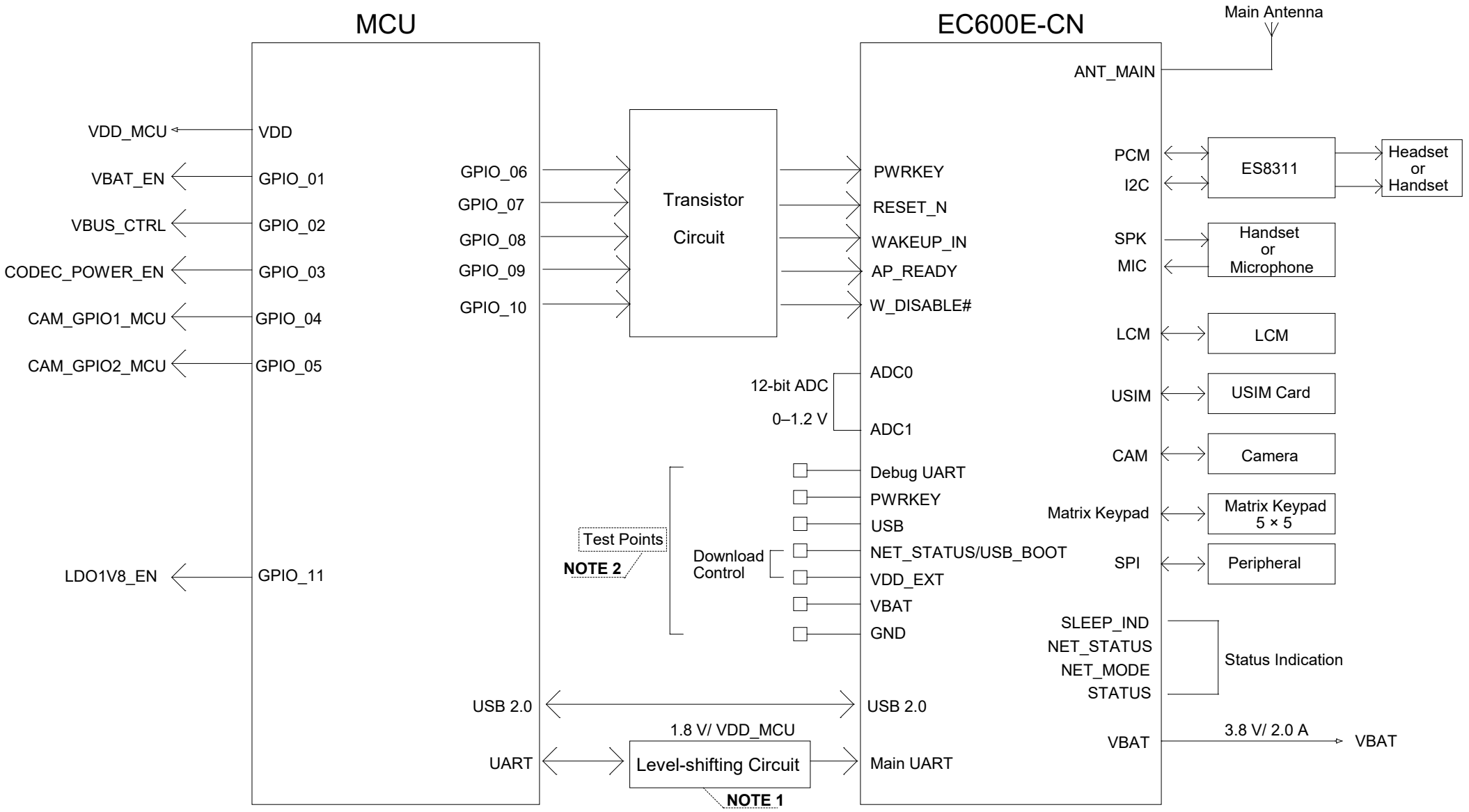
1.1. Introduction

This document provides the reference design for Quectel EC600E-CN QuecOpen® module. The reference design mainly includes block diagrams of power supply, USIM interface, UART interfaces, LCM interface, camera interface, antenna interface, SPI interface, matrix keypad interface, audio codec design, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.
2. Test points of USB_VBUS, USB_DP/DM, NET_STATUS/USB_BOOT and VDD_EXT must be reserved. It is recommended to reserve the test points of DBG_TXD/RXD, PWRKEY and VBAT_BB/RF.
3. Analog audio interface (pins 21–25), LCM interface (pins 62–67), WAKEUP_IN (pin 49), CAM_VDD (pin 17) and CAM_VDDIO (pin 68) are optional.

   If you need these functions, please contact Quectel Technical Support.

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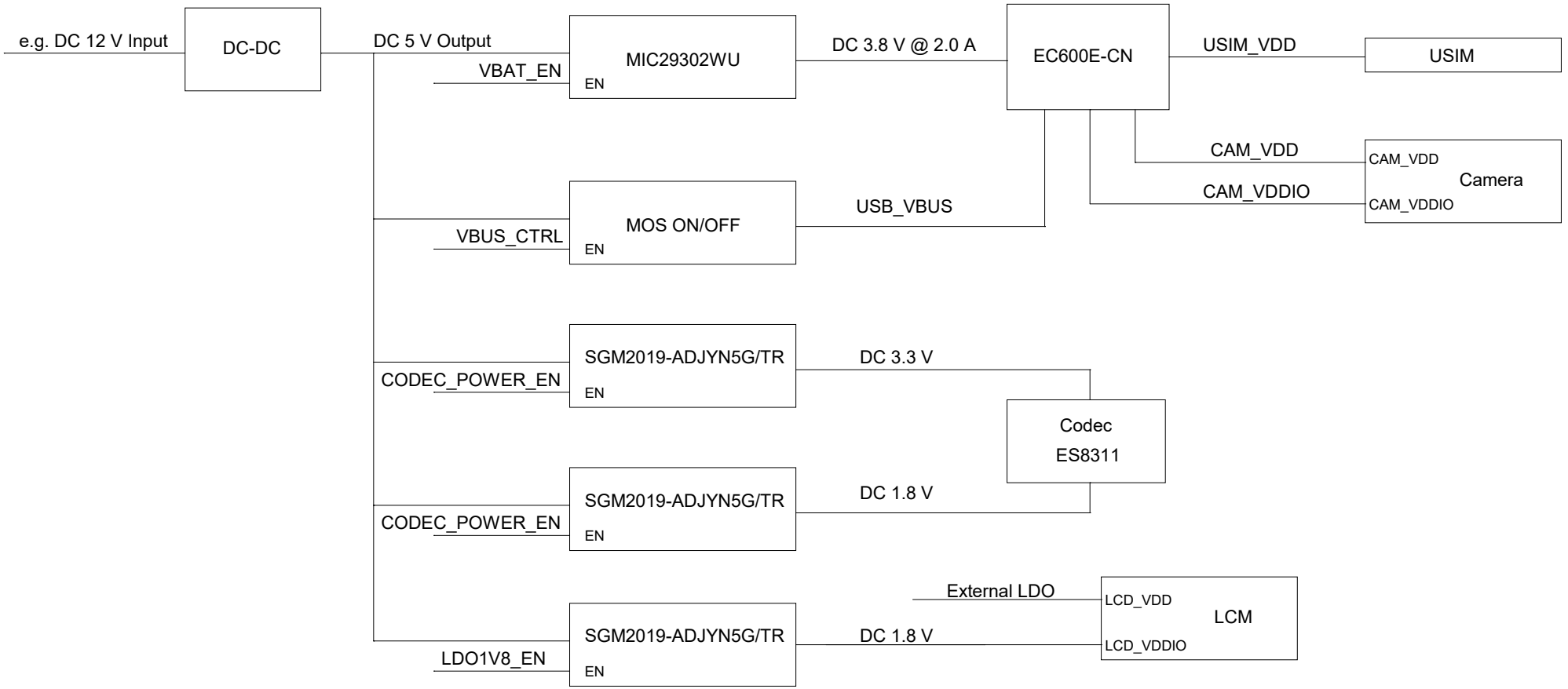
DATE: Friday, July 14, 2023	SHEET: 1 OF 16	

Power System Block Diagram



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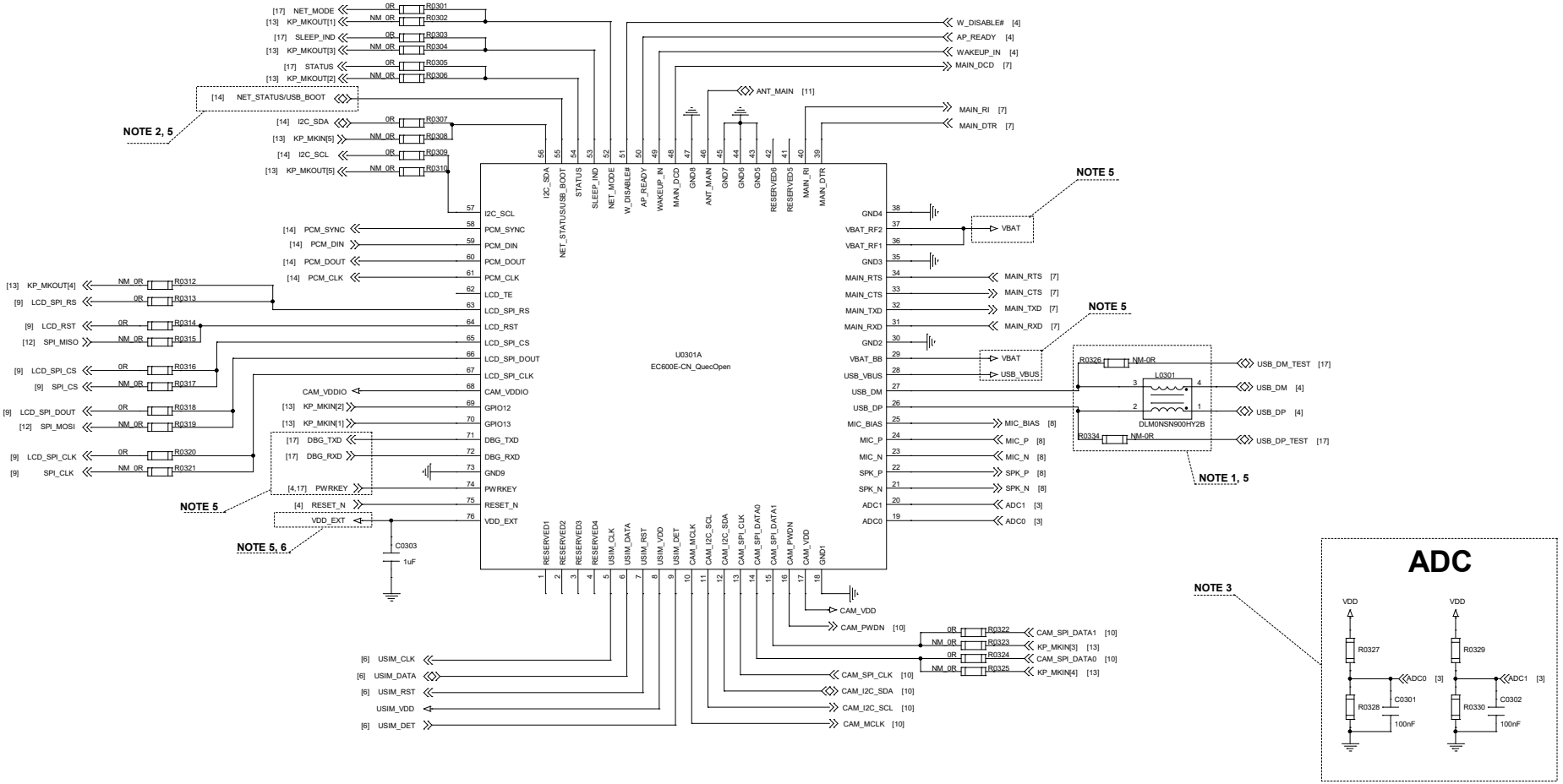
DATE: Friday, July 14, 2023	SHEET: 2 OF 16	

Module Interfaces



NOTE:

1. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission, and it should be placed close to the module.

   Meanwhile, test points of USB interface must be reserved, which can be used for firmware upgrading, software debugging and log output to analyze your problems. Keep extra stubs of the trace as short as possible.

   The two resistors R0326 and R0334 should be placed close to the module to ensure the integrity of the USB signals.

2. If the module does not need to enter emergency download mode, NET_STATUS/USB_BOOT cannot be pulled up to high level before the module successfully starts up.

3. The voltage input range of ADC0 and ADC1 interfaces is 0–1.2 V. When the acquisition voltage is larger than 1.2 V, it is recommended to use a resistor divider circuit.

   The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for design.

4. Ensure there is a complete reference ground plane below the module, and the gound plane should be placed as close to the module layer as possible.

   Other traces cannot be routed on the first layer below the module, and at least four-layer board design is recommended.

5. Test points of USB_VBUS, USB_DP/DM, NET_STATUS/USB_BOOT and VDD_EXT must be reserved. It is recommended to reserve the test points of DBG_TXD/RXD, PWRKEY and VBAT_BB/RF.

6. Pins with wake-up interrupt: WAKEUP_IN, MAIN_DTR, MAIN_RXD, AP_READY, W_DISABLE#, USIM_DET, USB_VBUS.

   For the version that VDD_EXT is powered down in sleep mode, these pins cannot be pulled up to VDD_EXT.

7. All GND pins should be connected to the ground, and keep unused and RESERVED pins unconnected.

8. For details of GPIO multiplexing function, refer to *Quectel_EC600E-CN_QuecOpen_GPIO_Configuration*.

9. Analog audio interface (pins 21–25), LCM interface (pins 62–67), WAKEUP_IN (pin 49), CAM_VDD (pin 17), CAM_VDDIO (pin 68), GPIO12 (pin 69), GPIO13 (pin 70) are optional. If you need these functions, please contact Quectel Technical Support.

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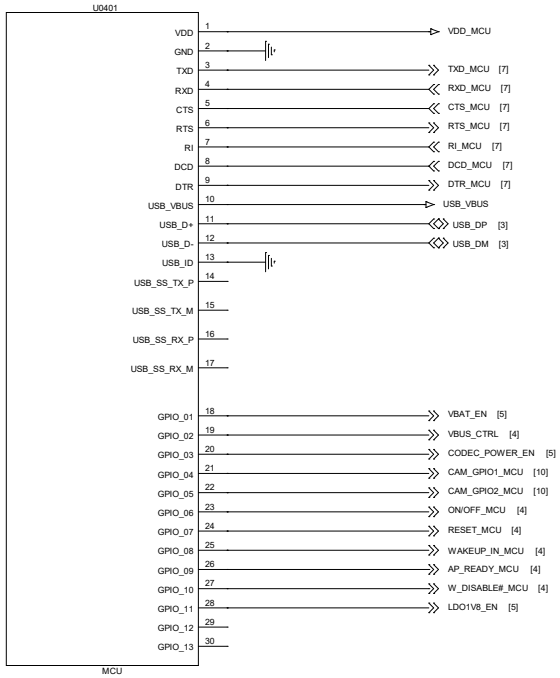
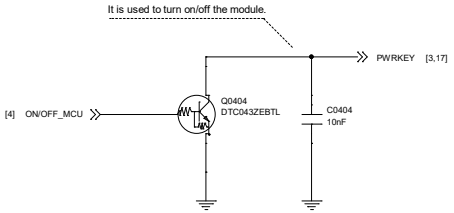
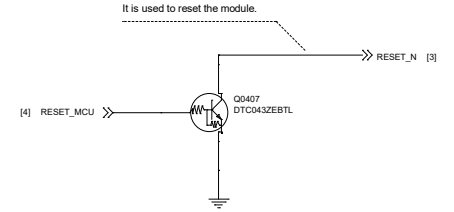
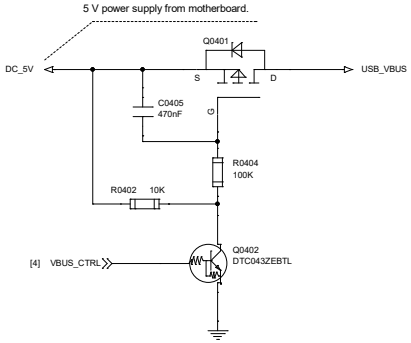
DATE: Friday, July 14, 2023	SHEET: 3 OF 16	

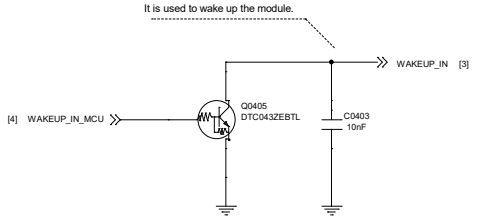
MCU Interfaces

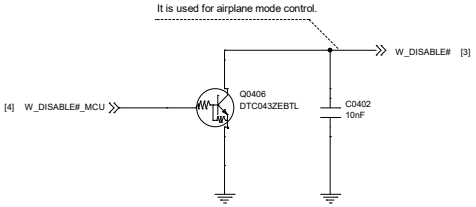


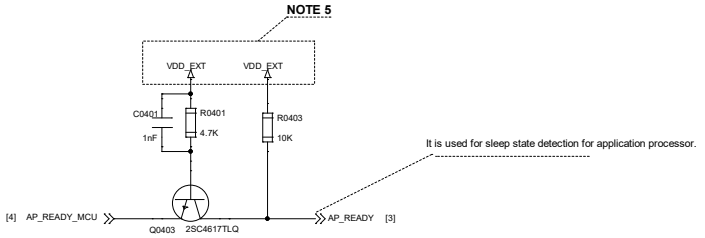












NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB interface of the module can only serve as a slave device and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL of MCU is used to turn on/off the power supply of USB_VBUS.
3. The reset function of the module requires the PWRKEY and RESET_N pins to work together. See the hardware design document of the module.
4. It is recommended to select the MCU's default lower-level GPIO pins as the control pins for the module's PWRKEY and RESET_N pins. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.
5. For the version that VDD_EXT is powered down in sleep mode, this pull-up power supply needs to be replaced with an external 1.8 V power supply.

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PROJECT: EC600E-CN QuecOpen		VER: 1.0
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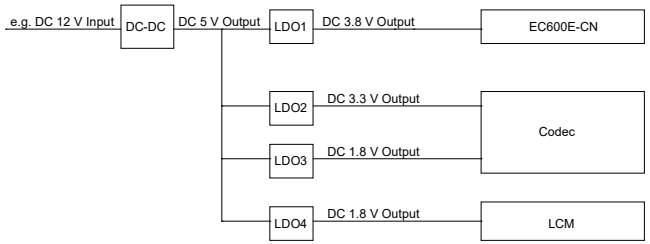
DATE: Friday, July 14, 2023	SHEET: 4 OF 16	

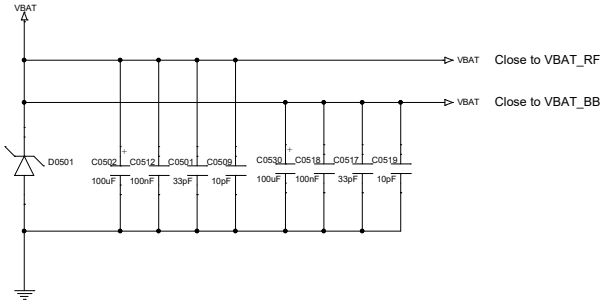
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to a 5.0 V voltage. and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, Codec and LCM.



VBAT Design

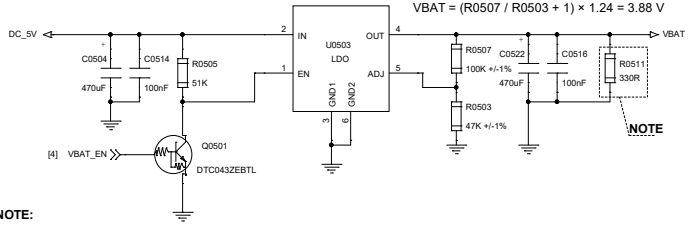


NOTE:

1. The power supply should be able to provide sufficient current of at least 2.0 A for the module.
2. The width of VBAT_BB trace should be not less than 1 mm, and the width of each VBAT_RF trace should be not less than 2 mm.
3. The recommended operating voltage of VBAT ranges from 3.3 V to 4.3 V, and the typical value is 3.8 V.

LDO Application

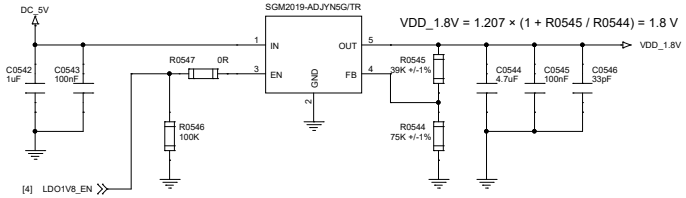
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



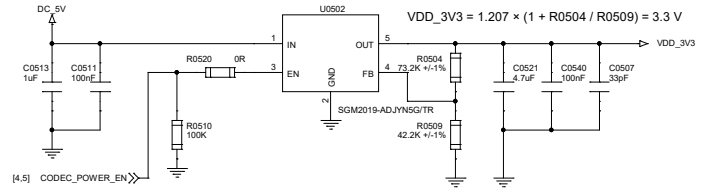
NOTE:

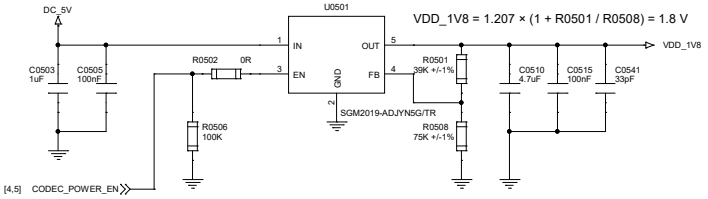
The recommended load current should be larger than 10 mA.

Power Supply for LCM



Power Supply for Codec





NOTE:

1. CODEC_POWER_EN is used to turn on/off VDD_1V8 and VDD_3V3.
2. To ensure the audio Codec ES8311 works normally, the power-up/down interval between VDD_1V8 and VDD_3V3 power supplies should not exceed 10 ms.

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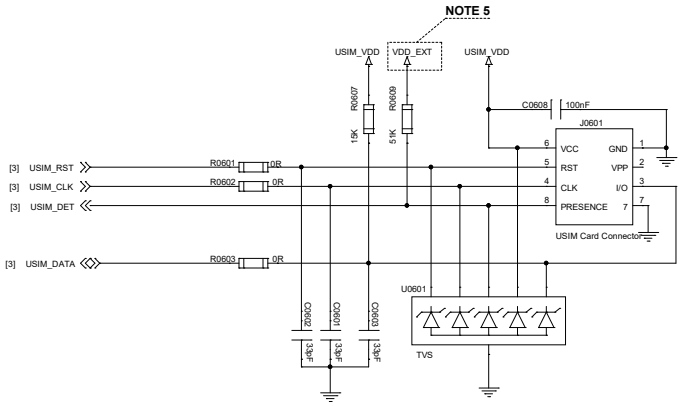
PROJECT: EC600E-CN QuecOpen	VER: 1.0	
DRAWN BY: Fanny CHEN	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 5 OF 16	

USIM Interface Design

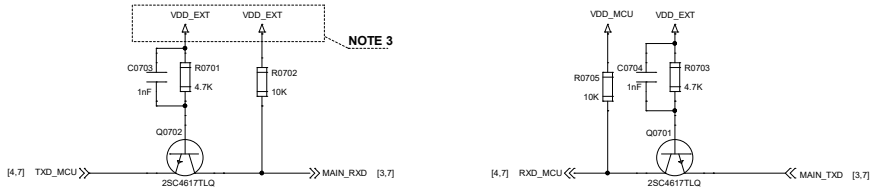


NOTE:

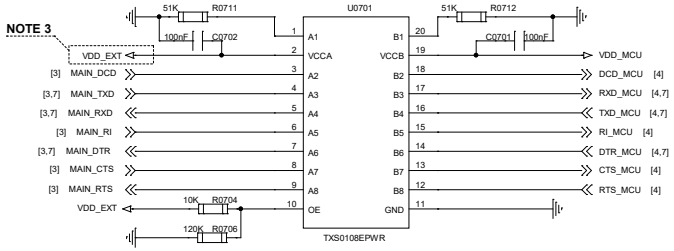
1. It is recommended to use U0601 to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistor R0607 can improve the anti-jamming capability, and should be placed close to the USIM card connector.
3. R0601–R0603 are used for debugging, and C0601–C0603 are used for filtering out RF interference.
4. The capacitance of C0608 should be less than 1 μF and it should be placed close to the USIM card connector.
5. For the version that VDD_EXT is powered down in sleep mode, the pull-up power supply of USIM_DET needs to be connected to an external 1.8 V power supply.
   For the version that VDD_EXT is not powered down in sleep mode, the pull-up power supply of USIM_DET can be connected to VDD_EXT.

UART Interface Design

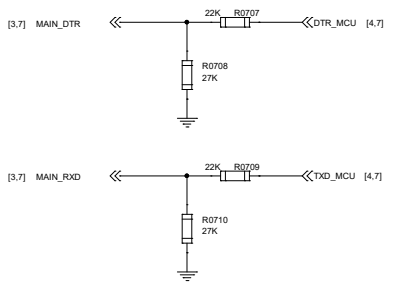
UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



Resistor Divider Circuit



NOTE:

1. There are two level-shifting circuits: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0108EPWR.
3. For the version that VDD_EXT is not powered down in sleep mode, the pull-up power supply of MAIN_RXD and VCCA can be connected to VDD_EXT.

   For the version that VDD_EXT is powered down in sleep mode, VDD_EXT cannot be used as the pull-up power supply for MAIN_RXD and MAIN_DTR.

   So there are two options to choose from:

   a. Use an external 1.8 V power supply instead of VDD_EXT to connect to the pull-up power supply of MAIN_RXD and VCCA.

   b. MAIN_RXD and MAIN_DTR should be designed with resistor divider circuit. Pay attention to adjusting the resistance value of R0707–R0710 according to the actual situation.
4. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0703 and C0704 of 1 nF can improve the signal quality.
5. If the level of the external host is 1.8 V and the module's MAIN_RXD and MAIN_TXD are directly connected to the host's TXD and RXD, the MAIN_TXD of the module should be pulled up to 1.8 V via a 10 kΩ resistor to prevent the host from receiving error messages when the module is in sleep mode.

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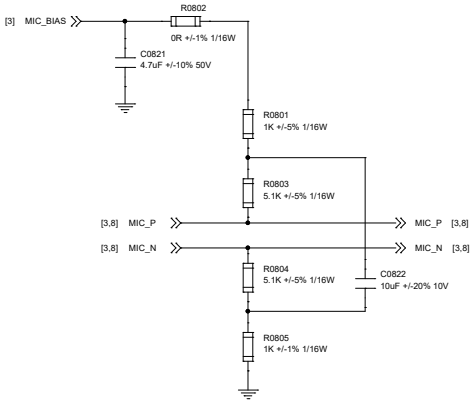
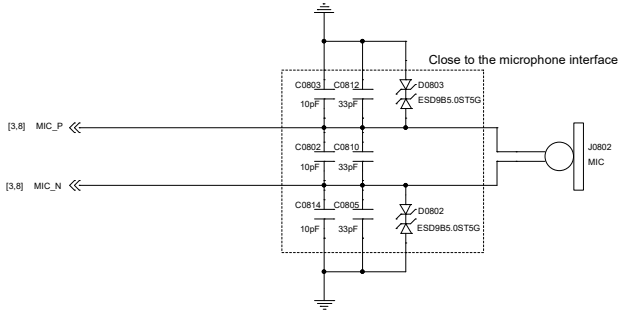
PROJECT: EC600E-CN QuecOpen		VER: 1.0
DRAWN BY: Fanny CHEN	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 7 OF 16	

Analog Audio Design

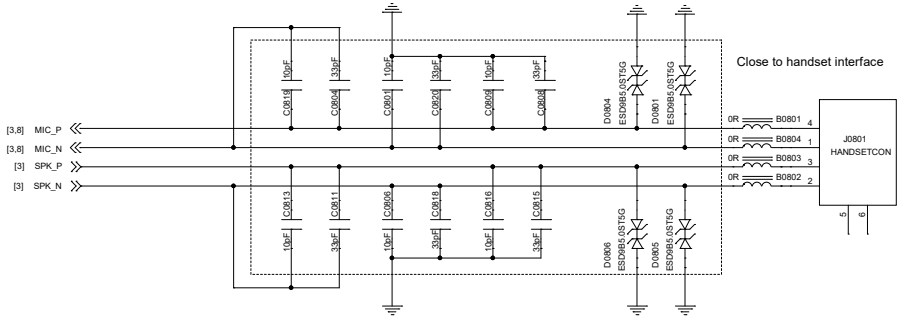
Microphone Bias Circuit



Microphone Application



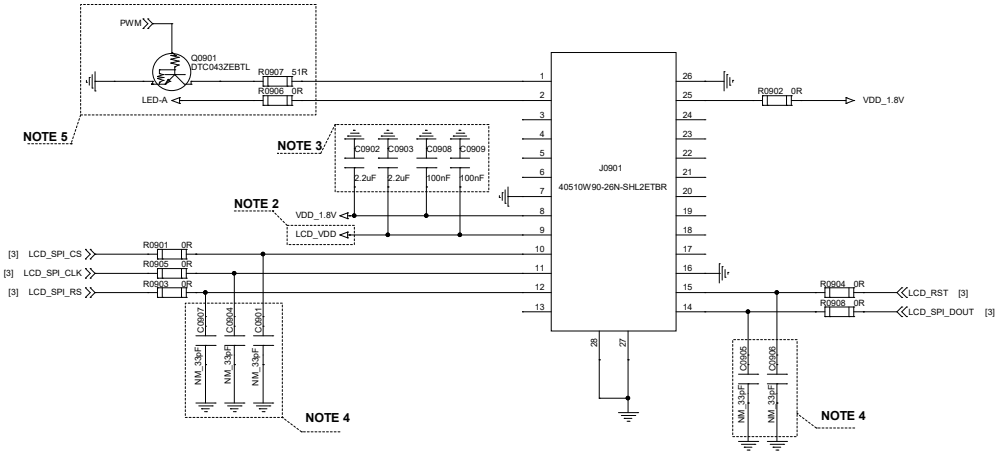
Handset Application



NOTE:

1. The analog audio interface (pins 21–25) is optional. If you need this function, please contact Quectel Technical Support.
2. Both the MIC and SPK signal traces need to be routed as differential pairs.
3. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise signals.
4. In the analog audio design, you can choose either the analog audio or the Codec. It is not necessary to select both.
5. It is recommended to use 10 pF and 33 pF capacitors to filter TDD noise.
6. The design of this page is only applicable to the module with built-in Codec.

LCM Interface Design



NOTE:

1. The LCM interface (pins 62–67) is optional. If you need this function, please contact Quectel Technical Support.
2. It is recommended to design the power supply of LCM interface by yourself.
3. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.
4. The 33 pF capacitors of the signal pins should be reserved, and can be used according to the actual debugging situation.
5. The LED-A backlight power supply is designed by youself, and you can select the approriate resistor (R0907) according to the MOSFET rated current and LED-A voltage value.

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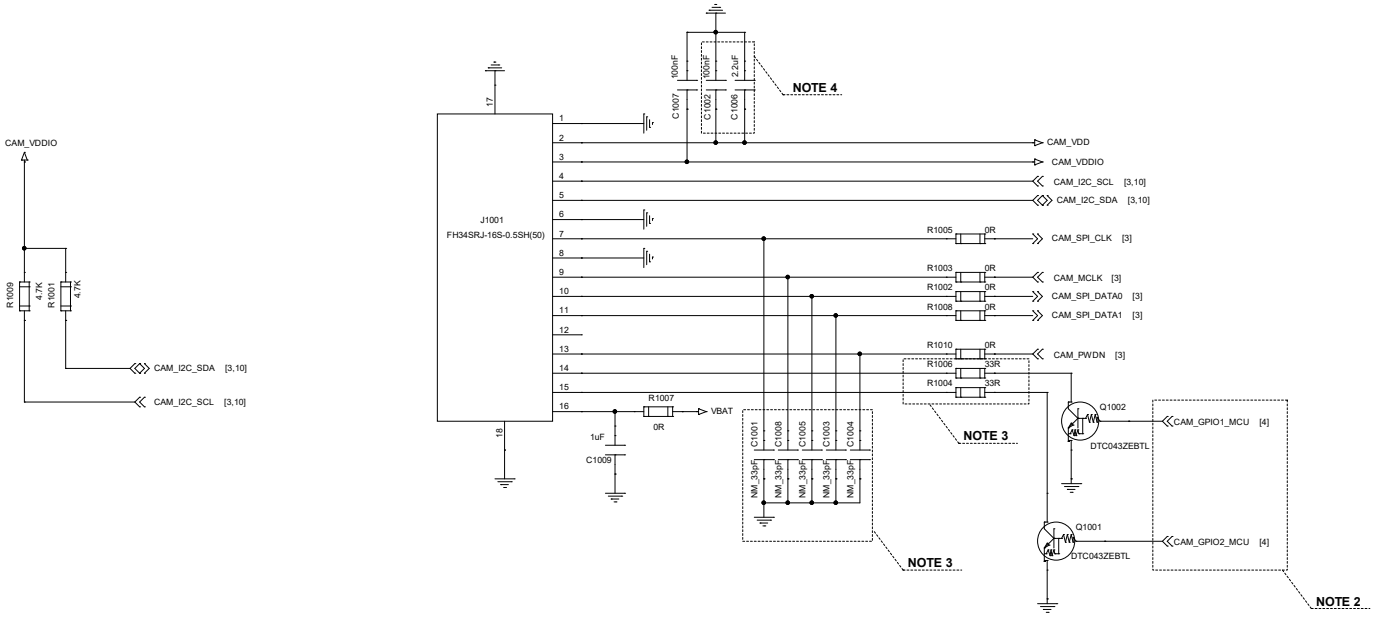
PROJECT: EC600E-CN QuecOpen		VER: 1.0
DRAWN BY: Fanny CHEN	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 9 OF 16	

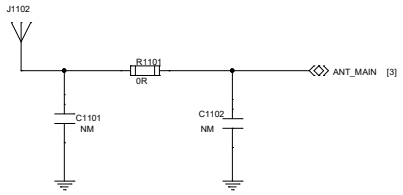
Camera Interface Design



NOTE:

1. CAM_VDD (pin 17) and CAM_VDDIO (pin 68) are optional. If you need these functions, please contact Quectel Technical Support.
2. By controlling the triode switching circuit, the CAM_GPIO1_MCU pin controls the cathode of the positioning light of the camera, and the CAM_GPIO2_MCU pin controls the cathode of the supplement light of the camera.
   It is recommended to select default pull-down GPIO pins as the two control pins.
3. The 33 pF capacitors of the signal pins should be reserved, and can be used according to the actual debugging situation.
   The values of current limiting resistors of positioning light and supplement light (R1004 and R1006) should be varied according to the required brightness.
4. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly. Otherwise, the power supply noise may lead to abnormalities such as white dots on the preview screen.

Antenna Interface Design

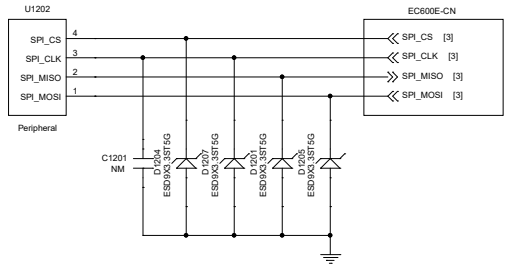


NOTE:

1. Use a Π-type matching circuit for the antenna interface.
2. The single-ended impedance of the RF antenna is 50 Ω, and keep the traces as short as possible.

Quectel Wireless Solutions		
PROJECT: EC600E-CN QuecOpen		VER: 1.0
DRAWN BY: Fanny CHEN	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 11OF 16	

SPI Interface Design (Master Mode)

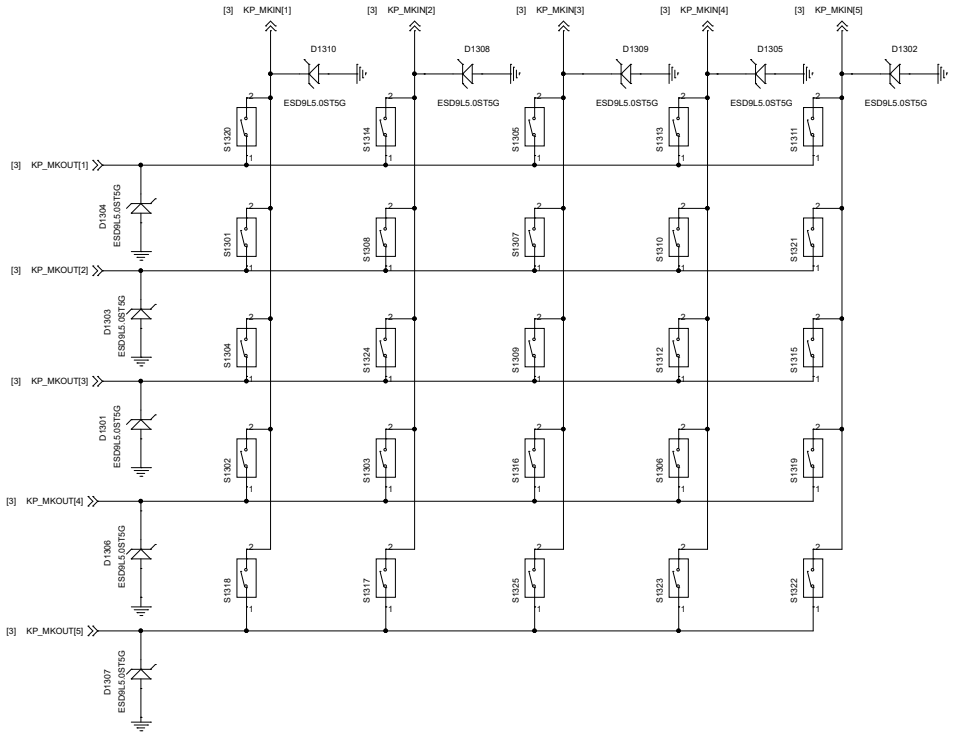


NOTE:

The SPI interface is multiplexed from LCD_RST, LCD_SPI_CS, LCD_SPI_DOUT and LCD_SPI_CLK.

Quectel Wireless Solutions		
PROJECT: EC600E-CN QuecOpen		VER: 1.0
DRAWN BY: Fanny CHEN	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 12OF 16	

Matrix Keypad Interface Design



NOTE:

The matrix keypad interface is multiplexed from GPIO13, NET_MODE, GPIO12, STATUS, CAM_SPI_DATA1, SLEEP_IND, CAM_SPI_DATA0, LCD_SPI_RS, I2C_SDA and I2C_SCL.

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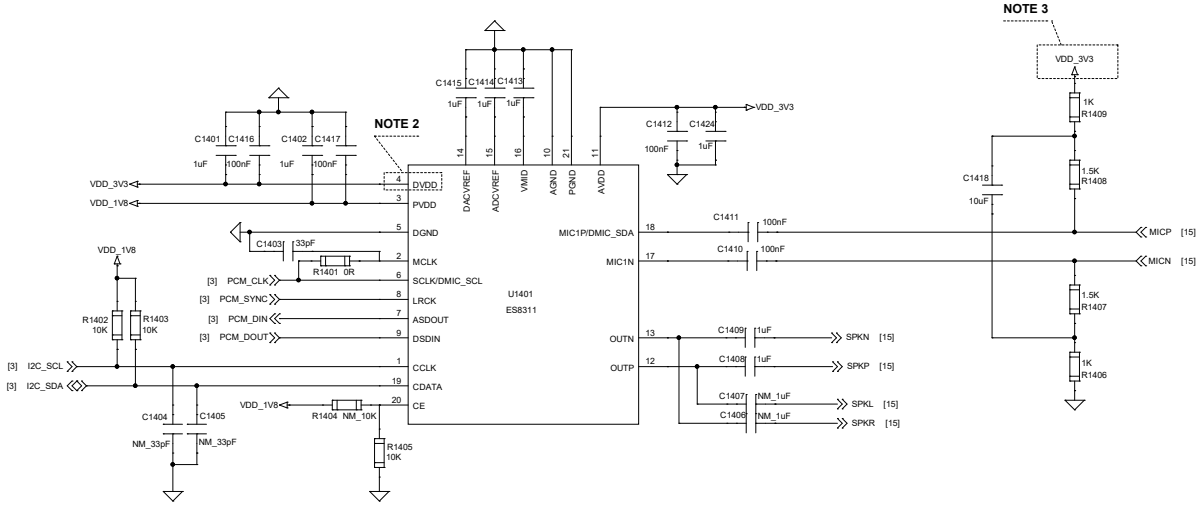
DATE: Friday, July 14, 2023	SHEET: 13OF 16	

Audio Codec Design (ES8311)



NOTE:

1. ES8311 power-up/down sequence: AVDD, PVDD and DVDD are powered on and off at the same time, or with the interval within 10 ms.
2. When the sampling frequency is 8 kHz and the clock frequency is 512 kHz, DVDD must be connected to 1.8 V.
3. The bias voltage needs to be stable and the ripple should be as small as possible.
4. Please pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805.
   For more details, see the sheet of Audio Codec Interface Design.
5. For more details, see the datasheet of ES8311.

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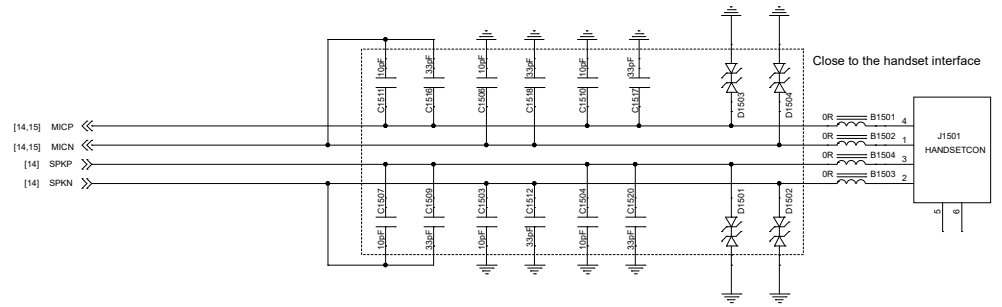
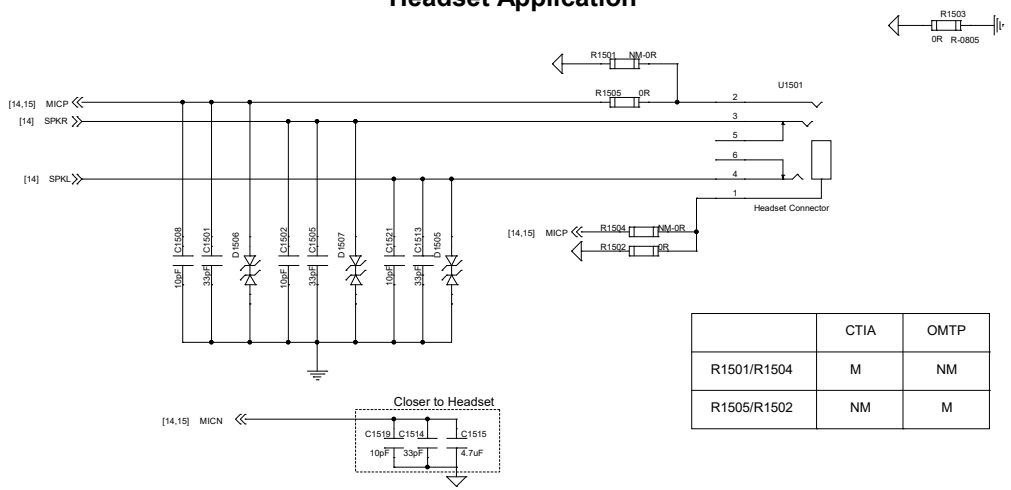
DATE: Friday, July 14, 2023	SHEET: 14OF 16	

Audio Codec Interface Design

Handset Application



Headset Application



	CTIA	OMTP
R1501/R1504	M	NM
R1505/R1502	NM	M

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset applications, route the MIC and SPK signal traces as differential pairs respectively.
3. In headset applications, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces shall be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.
5. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (short-circuit through single point grounding).

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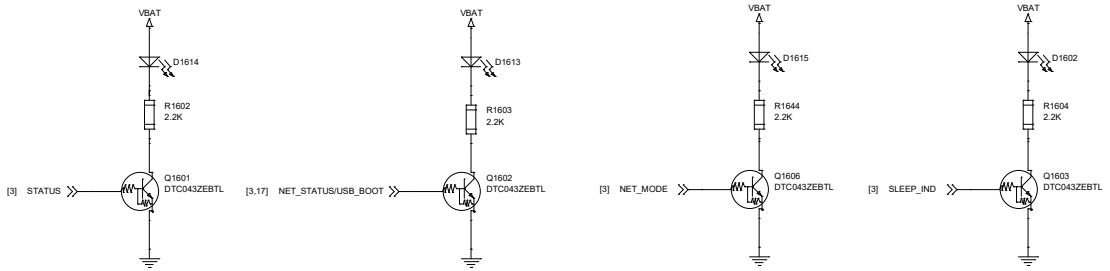
DATE: Friday, July 14, 2023	SHEET: 15OF 16	

Other Designs

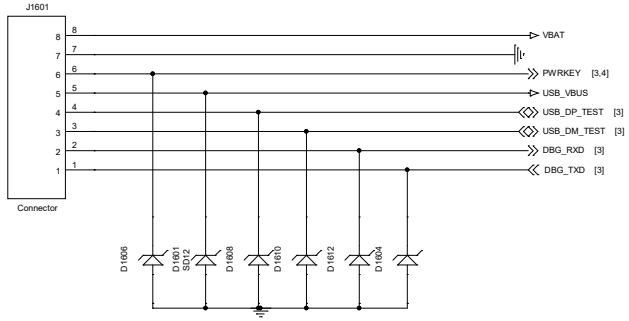
Indicators



NOTE:

1. For more details about STATUS, NET_STATUS/USB_BOOT, NET_MODE and SLEEP_IND, see the hardware design document of the module.
2. If the low power consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS, NET_STATUS/USB_BOOT, NET_MODE and SLEEP_IND indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

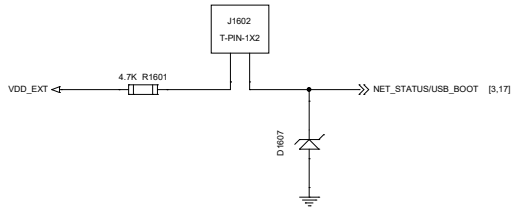
Reserved Test Points



NOTE:

1. Test points of USB_VBUS, USB_DP/DM, NET_STATUS/USB_BOOT and VDD_EXT must be reserved. It is recommended to reserve the test points of DBG_TXD/RXD, PWRKEY and VBAT_BB/RF.
2. Test points of USB interface can be used for firmware upgrade, software debugging and log output to analyze your problems.
3. The parasitic capacitance of the ESD protection components on USB data traces should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

USB_BOOT Interface



NOTE:

1. Ensure to reserve the NET_STATUS/USB_BOOT interface design and a test point must be reserved for NET_STATUS/USB_BOOT.
2. Pull up NET_STATUS/USB_BOOT to VDD_EXT before the module starts up, and the module will enter emergency download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

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DATE: Friday, July 14, 2023	SHEET: 16OF 16	