BG770S-GL

Hardware Design

LPWA Products

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Quectel Wireless Solutions Co., Ltd.
No. 8 Waipojing Road, Sijing Town, Songjiang District, Shanghai 201601, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
https://www.quectel.com/contact/.

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2025-07-11	Kok Hoong Yu/ Mior Abdullah Bin Mior Ahmad Nasarudin/ Hyde Yang	Creation of the document
1.0	2025-11-20	Kok Hoong Yu/ Mior Abdullah Bin Mior Ahmad Nasarudin/ Hyde Yang	First official release
1.1	2026-02-02	Muhammad Nabil Irfan Bin Mohammad Amin/ Mior Abdullah Bin Mior Ahmad Nasarudin/ Hyde Yang	1. Added a description specifying that TVS should be added to avoid causing damage to the module (Chapter 3.8.2). 2. Updated the power consumption data under Rock Bottom and Sleep Mode conditions (Table 39).

Contents

Table Index

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1 Introduction

This document defines BG770S-GL modules and describes its air interface and hardware interfaces which connect with your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and to set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an embedded IoT wireless communication module. It provides data connectivity on LTE HD-FDD network. It also provides GNSS functionality to meet your specific application demands.

The module is based on an architecture in which WWAN (LTE) and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. Please see ***document [1]*** for more details.

BG770S-GL is compliant with 3GPP Release 14 and is capable of supporting 3GPP Releases 15–17 through a software upgrade.

The module is an industrial-grade module for industrial and commercial applications only.

Table 2: Basic Information

BG770S-GL	
Packaging type	LGA
Pin counts	94
Dimensions	(14.9 +0.3/-0.15) mm × (12.9 +0.3/-0.15) mm × (1.9 ±0.2) mm
Weight	Approx. 0.8 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and GNSS Types of the Module

Module	Supported Bands	Power Class	GNSS
BG770S-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B26/B27/B28/B66/B85 **Cat NB2:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66/B85	Power Class 3 (23 dBm ±2 dB)	GPS, GLONASS*

NOTE

The module supports the above frequency bands in hardware, but actual applications may be subject to local regulations.

With a compact profile of 14.9 mm × 12.9 mm × 1.9 mm, the module can fit most applications.

The module is an SMD type module which can be embedded into applications through its 94 LGA pins. It supports internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for you to use these internet service protocols easily.

2.2. Key Features

Table 4: Key Features of BG770S-GL Module

Features	Details
Power Supply [1]	● VBAT_BB: 2.2–4.35 V, typ. 3.3 V ● VBAT_RF: 3.1–4.3 V, typ. 3.3 V
Transmit Power	Class 3 (23 dBm ±2 dB) for LTE HD-FDD bands

[1] When the module is turned on normally, in order to ensure full functionality mode, the minimum power supply voltage should be at least 3.1 V.

LTE Features	● Supports 3GPP Rel-14 (LTE Cat M1 and LTE Cat NB2) ● Supports minimum 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB2 ● Data Rate (Max.): - Cat M1: 588 kbps (DL)/1119 kbps (UL) - Cat NB2: 127 kbps (DL)/158 kbps (UL)
Internet Protocol Features	● Supports TCP/PPP/UDP/SSL/MQTT/FTP(S)/HTTP(S)/LwM2M*/IPv4/IPv6/TLS/DTLS/PING/CoAP*/NITZ protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interface	● Supports 1.8 V external USIM/eSIM card only ● USIM/eSIM cannot be used simultaneously
UART Interfaces	**Main UART:** ● Used for data transmission and AT command communication, GNSS data and NMEA sentences output ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for firmware upgrade, software debugging, FW log output, and RF calibration ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control
PCM Interface*	Supports one digital audio interface: PCM interface for VoLTE*
I2C Interface*	Supports one I2C master interface
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Network Status Indication	One NET_STATUS pin for network activity status indication
Status Indication	One STATUS pin for the operation status indication
GNSS Features	● Supports GPS, GLONASS* ● Protocol: NMEA 0183 ● Data update rate: 1 Hz ● Supports AGNSS
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS)

Temperature Range	● Normal operating temperature: -35 °C to +75 °C [2] ● Extended operating temperature: -40 °C to +85 °C [3] ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● UART ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[2] Within the operating temperature range, the module's indicators comply with 3GPP specification requirements.
[3] Within the range of -40 to -35 °C or 75 to 85 °C, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The following figure shows a block diagram of the BG770S-GL module and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

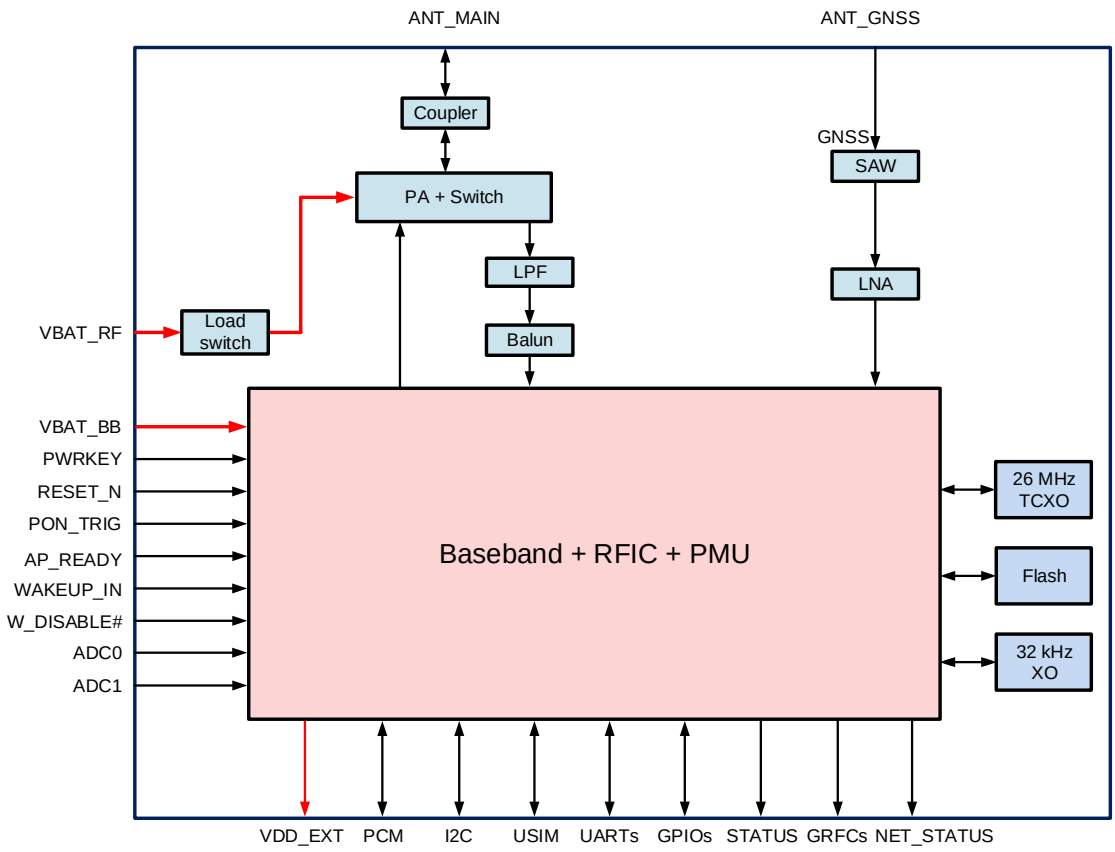


Figure 1: Functional Diagram of BG770S-GL

NOTE

BG770S-GL's baseband chip includes an MRAM (Magnetoresistive Random Access Memory), a non-volatile memory that stores data using magnetic states. MRAM is sensitive to strong magnetic fields. Please refer to ***Chapter 6.7*** for more details about the MRAM magnetic field tolerance.

2.4. Pin Assignment

The following figure shows the pin assignment of the module.

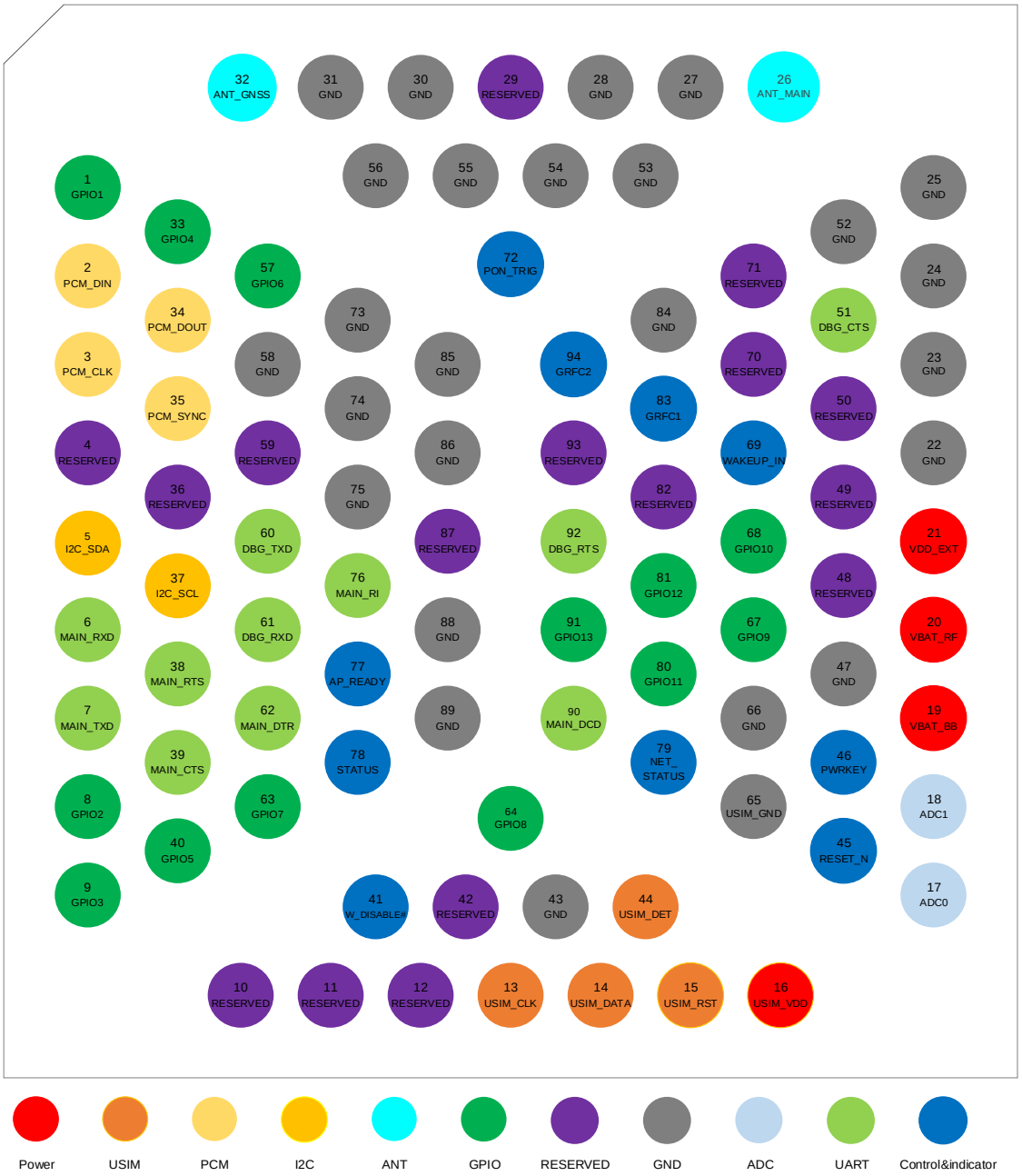


Figure 2: Pin Assignment (Top View)

NOTE

Connect GND pins to ground in the design.

2.5. Pin Definitions

Table 5: Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pulled Up
PD	Pulled Down
Hi-Z	High Impedance

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	19	PI	-	Power supply for the module's baseband part	Vmax = 4.35 V Vmin = 2.2 V Vnom = 3.3 V	A test point is recommended to be reserved.
VBAT_RF	20	PI	-	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.1 V Vnom = 3.3 V	A test point is recommended to be reserved.

VDD_EXT	21	PO	-	Provide 1.8 V for external circuit	Vmax = 1.872 V Vmin = 1.728 V Vnom = 1.8 V $I_O$max = 50 mA	If this pin is unused, keep it open. A test point is recommended to be reserved.
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89					Connect these pins to ground.
Turn On/Off						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	46	DI	PU	Turn on/off the module	V_{IL}max = 0.2 V V_{IH}min = 0.6 V	Internally pulled up. Active low. A test point is recommended to be reserved.
Reset						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
RESET_N	45	DI	PU	Reset the module	V_{IL}max = 0.2 V V_{IH}min = 0.6 V	Internally pulled up. Active low. A test point is recommended to be reserved if unused.
Status Indication						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
STATUS	78	DO	PD	Indicate the module's operation status	VDD_EXT	Internally pulled down. 1.8 V power domain. If this pin is unused, keep it open.
NET_ STATUS	79	DO	Hi-Z	Indicate the module's network activity status		1.8 V power domain. If this pin is unused, keep it

						open.
USIM Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	44	DI	Hi-Z	USIM card hot-plug detect	VDD_EXT	1.8 V power domain. If this pin is unused, keep it open.
USIM_VDD	16	PO	-	USIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Supports 1.8 V USIM card only.
USIM_RST	15	DO	PD	USIM card reset	VDD_EXT	1.8 V power domain.
USIM_DATA	14	DIO	Hi-Z	USIM card data		
USIM_CLK	13	DO	PD	USIM card clock		
USIM_GND	65	-	-	Dedicated ground for USIM card	-	Connect this pin to ground.
Main UART Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	62	DI	Hi-Z	Main UART data terminal ready	VDD_EXT	1.8 V power domain. If these pins are unused, keep them open.
MAIN_RXD	6	DI	Hi-Z	Main UART receive		
MAIN_TXD	7	DO	Hi-Z	Main UART transmit		
MAIN_CTS	39	DO	PU	Clear to send signal from the module		Connect to MCU's CTS. 1.8 V power domain. If these pins are unused, keep them open.
MAIN_RTS	38	DI	Hi-Z	Request to send signal to the module		Connect to MCU's RTS. 1.8 V power domain. If these pins are

						unused, keep them open.
MAIN_DCD	90	DO	Hi-Z	Main UART data carrier detect		1.8 V power domain. If these pins are unused, keep them open.
MAIN_RI	76	DO	Hi-Z	Main UART ring indication		
Debug UART Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	61	DI	Hi-Z	Debug UART receive	VDD_EXT	1.8 V power domain. Test points must be reserved. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
DBG_TXD	60	DO	Hi-Z	Debug UART transmit		
DBG_CTS	51	DO	Hi-Z	Clear to send signal from the module		
DBG_RTS	92	DI	Hi-Z	Request to send signal to the module		
I2C Interface*						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	37	OD	PD	I2C serial clock	Vmax = 1.872 V Vmin = 1.728 V Vnom = 1.8 V $I_O$max = 50 mA	External pull-up resistors are required. 1.8 V only. If unused, keep these pins open.
I2C_SDA	5	OD	PD	I2C serial data		
PCM Interface*						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	35	DIO	Hi-Z	PCM data frame sync	VDD_EXT	In master mode, they are output signals. In slave
PCM_CLK	3	DIO	PD	PCM clock		

						mode, they are input signals. If unused, keep these pins open.
PCM_DIN	2	DI	PD	PCM data input		If unused, keep these pins open.
PCM_DOUT	34	DO	Hi-Z	PCM data output		
Antenna Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	26	AIO	-	Main antenna interface		50 Ω impedance.
ANT_GNSS	32	AI	-	GNSS antenna interface		50 Ω impedance. If this pin is unused, keep it open.
GPIO Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
GPIO1	1	DIO	Hi-Z	General-purpose input/output	VDD_EXT	1.8 V power domain. If these pins are unused, keep them open. Test points are recommended to be reserved.
GPIO2	8	DIO	Hi-Z			
GPIO3	9	DIO	Hi-Z			
GPIO4	33	DIO	Hi-Z			
GPIO5	40	DIO	Hi-Z			
GPIO6	57	DIO	PU			
GPIO7	63	DIO	PU			
GPIO8	64	DIO	Hi-Z			1.8 V power domain. If these pins are unused, keep them open. Test points are recommended to be reserved.
GPIO9	67	DIO	Hi-Z			
GPIO10	68	DIO	PD			
GPIO11	80	DIO	Hi-Z			
GPIO12	81	DIO	Hi-Z			

GPIO13	91	DIO	Hi-Z			
ADC Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
ADC0	17	AI	-	General-purpose ADC interface	Input voltage range: 0–1.8 V	If these pins are unused, keep them open. Test points are recommended to be reserved.
ADC1	18	AI	-	General-purpose ADC interface		
Other Interface Pins						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	41	DI	Hi-Z	Airplane mode control	VDD_EXT	1.8 V power domain. Pulled up by default. When this pin is at low level, the module enters airplane mode. If this pin is unused, keep it open.
WAKEUP_IN*	69	DI	-	Wake up the module	V_{IL}min = -0.2 V V_{IL}max = 0.2 V V_{IH}min = 0.6 V V_{IH}max = 1.98 V	A test point is recommended to be reserved.
AP_READY	77	DI	Hi-Z	Application processor ready	VDD_EXT	1.8 V power domain. If this pin is unused, keep it open.
PON_TRIG	72	DI	PD	Wake up the module from PSM	V_{IL}min = -0.2 V V_{IL}max = 0.2 V V_{IH}min = 0.6 V V_{IH}max = 1.98 V	Internally pulled down by default. If unused, keep this pin open. A test point is recommended to

						be reserved.
GRFC Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Hi-Z	Generic RF controller	VDD_EXT	1.8 V power domain. If these pins are unused, keep them open. Test points are recommended to be reserved.
GRFC2	94	DO	Hi-Z	Generic RF controller		
RESERVED Pins						
Pin Name	**Pin No.**					**Comment**
RESERVED	4, 10–12, 29, 36, 42, 48–50, 59, 70,71, 82, 87, 93					Keep these pins open.

NOTE

1. When the module is turned on normally, in order to ensure full functionality mode, the minimum power supply voltage should be at least 3.1 V. Every time VBAT is powered up or reconnected to the power source, the slew rate of VBAT should be less than 25 mV/μs.
2. ADC input voltage must not exceed 1.8 V.
3. Keep all RESERVED pins and unused pins unconnected.
4. After entering PSM or turn-off mode, it is prohibited to provide any external voltage to the module's I/O ports that are not defined as a wake-up source.
5. To reduce the probability of module damage and extend module service life, do not power up and down frequently.

2.6. TE-B Kit

Quectel supplies an evaluation board (BG770S-GL TE-B) with accessories to develop and test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Data	The module is connected to network. Its power consumption varies with the network setting and data transmission rate.
	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module into airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and USIM card are invalid.	
Sleep Mode	The module retains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption is reduced to an ultra-low level.	
Turn-off Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_BB and VBAT_RF) remains applied.	
Power Saving Mode (PSM)	PSM is similar to turn-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The power consumption is reduced to a minimized level.	
Recovery Mode	The module can burn firmware with an empty serial flash, or recover from firmware malfunction. For more details, see ***Chapter 3.7***.	

NOTE

For more details about **AT+CFUN**, please see ***document [3]***.

3.2. Low Power Mode

BG770S-GL module supports the following five power modes at the system layer:

- Active mode: Normal working mode.
- Sleep mode level 1: Has fast entry and recovery time and is mainly used during DRX networking mode.
- Sleep mode level 2: Has medium entry and recovery time and is mainly used during DRX and eDRX networking modes.
- Sleep mode level 3: Similar to sleep mode level 2 but offers lower power consumption due to unretained I/O logic.
- Shutdown mode: Provides the lowest system power, has long entry and recovery time and is mainly used for very long inactivity intervals like PSM.

NOTE

For more details about low power modes, please see ***document [4]***.

Table 8: Different Methods to Enter and Exit Low Power Modes

Low Power Type	Command	Requirements for Entering Sleep Mode	Wake-up Method
AT+QSCLK Command	**AT+QSCLK=1**	Pull down PON_TRIG while pulling up MAIN_DTR	● Pull up PON_TRIG ● Pull down MAIN_DTR ● Pull down PWRKEY for 256 ms–2 s and pull up
	AT+QSCLK=2	Pull down PON_TRIG while pulling up MAIN_DTR	● Pull up PON_TRIG ● Pull down MAIN_DTR ● Pull down PWRKEY for 256 ms–2 s and pull up
	AT+QSCLK=3	Pull down PON_TRIG and MAIN_DTR	● Pull up PON_TRIG ● Pull down PWRKEY for 256 ms–2 s and pull up

PSM	**AT+QPSMS=1,,,"<Requested_Periodic-TAU>","<Requested_Active-Time>"**	Pull down PON_TRIG	• Pull up PON_TRIG • Pull down PWRKEY for 256 ms–2 s and pull up
Turn off with PWRKEY	-	Pull down PWRKEY for 256 ms–2 s and pull up	• Pull down RESET_N • Pull down PWRKEY for 256 ms–2 s and pull up

NOTE

For details about the above AT commands, please see ***document [3]***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands correlative with RF function will be inaccessible. This mode can be set as follows:

Hardware:

W_DISABLE# is pulled up by default. Driving it low will make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both USIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled with **AT+QCFG="airplanecontrol"**. For details of the command, please see ***document [5]***.
2. The execution of **AT+CFUN=<fun>** may affect GNSS function. Since the module does not support concurrent operation of WWAN and GNSS, the GNSS function can be used when **<fun>**=0 or 4, but cannot be used when **<fun>**=1.
3. For more details about **AT+CFUN**, please see ***document [3]***.

3.4. Power Saving Mode (PSM)

The module minimizes its power consumption by entering PSM. The mode is similar to turn-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, in PSM the module cannot immediately respond to user requests.

When the module wants to use PSM, it shall request an Active Time value during every Attach and TAU procedure. If the network supports PSM use, it will allocate an Active Time value to the module to confirm PSM use. If the module wants to change the Active Time value, the module consequently requests the value it wants in the TAU procedure.

For BG770S-GL, if PSM is supported by the network, then it can be enabled via **AT+QPSMS**. In this case, driving PON_TRIG low will set the module to PSM. Any of the following methods can wake up the module from PSM:

- Driving PON_TRIG high and keeping it high will wake up the module from PSM.
- When the TAU timer expires, the module wakes up from PSM automatically.

NOTE

1. For details about **AT+QPSMS**, please see ***document [3]***.
2. PON_TRIG is pulled down by default.

3.5. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transmissions, and in particular, they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what were requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received

by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

3.5.1. e-I-DRX Sleep Mode

For BG770S-GL, if e-I-DRX is supported by the network, perform the steps below in sequence to let the module enter e-I-DRX sleep mode, in which case the data communication pins of the main UART interface are inaccessible.

1. Send **AT+CEDRXS=1** to enable e-I-DRX mode.
2. Send **AT+QSCLK=2** [4] to enable sleep mode.

To make the module exit e-I-DRX sleep mode, perform the steps below in sequence.

1. Send **AT+QSCLK=0** to disable sleep mode.
2. Send **AT+CEDRXS=0** to disable the use of e-I-DRX mode.

3.5.2. e-I-DRX Idle Mode

If e-I-DRX is supported by the network, just send **AT+CEDRXS=1** to make the module enter e-I-DRX idle mode, or send **AT+CEDRXS=0** to make the module exit e-I-DRX idle mode.

NOTE

1. After module enters sleep mode with **AT+QSCLK=3**, it is prohibited to provide any external voltage to the module's I/O ports that are not defined as a wake-up source.
2. For details about the above AT commands, please see ***document [3]***.

3.6. Sleep Mode

BG770S-GL can reduce its power consumption to an ultra-low value during the sleep mode. The following sub-chapters describe the power saving procedure.

3.6.1. UART Application Scenario

For BG770S-GL, if the MCU communicates with the module via the main UART interface, perform the steps below in sequence to make the module enter sleep mode, in which case the data communication pins of the main UART interface are inaccessible.

[4] Send either **AT+QSCLK=1** or **AT+QSCLK=2** or **AT+QSCLK=3** to enable sleep mode, and the last one is recommended for better power consumption performance. For more information of **AT+QSCLK**, please see ***document [3]***.

1. Drive PON_TRIG low.
2. Send **AT+CFUN=0** to set the module to minimum functionality mode. [5]
3. Drive MAIN_DTR low.
4. Execute **AT+QSCLK=2** [4] to enable sleep mode.
5. Drive MAIN_DTR high to enter sleep mode.

When the module is in sleep mode, perform the steps below in sequence to make the module exit sleep mode.

1. Drive MAIN_DTR low to wake up the module.
2. Execute **AT+QSCLK=0** to disable sleep mode.
3. Send **AT+CFUN=1** to set the module into full functionality mode.

The following figure shows the connection between the module and the MCU.

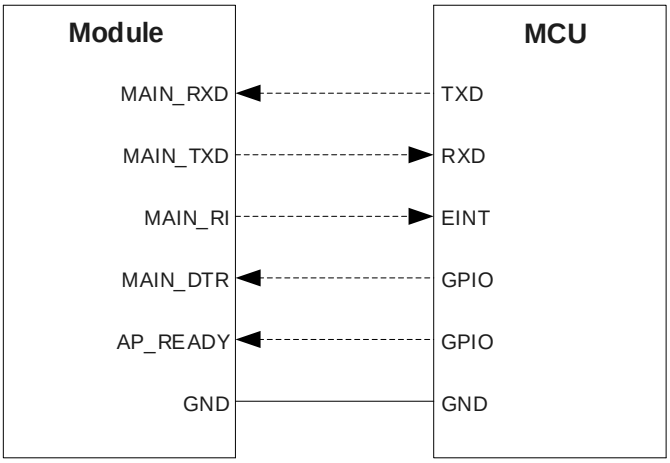


Figure 3: Sleep Mode Application via UART Interface

- When the module has a URC to report, MAIN_RI will wake up the MCU. See ***Chapter 4.3.3*** for details about MAIN_RI behavior.
- After the module is turned on, MAIN_DTR is internally pulled up by default.
- AP_READY will detect the sleep state of the MCU (it can be configured to detect high or low voltage levels). For details about **AT+QCFG="apready"**, please see ***document [5]***.

NOTE

Pay attention to the level match shown in the dotted line between the module and the MCU.

[5] After setting the module to minimum functionality with **AT+CFUN=0**, you can test the lowest power consumption of the module after the module enters sleep mode. If you need to keep the RF function on after the module enters sleep mode, there is no need to send any **AT+CFUN**. For more details about **AT+CFUN**, please see ***document [3]***.

3.7. Recovery Mode

The module features the recovery mode for firmware upgrade in emergency cases. Recovery mode can force the baseband chip of the module to upgrade firmware via debug UART interface.

The following steps in sequence can set the module to recovery mode for firmware upgrade.

1. Short-circuit DBG_TXD and DBG_RXD pins.
2. Drive PWRKEY low after VBAT has remained stable and in power-down mode for at least 400 ms to turn on the module. In this case the module will enter recovery mode.
3. After the module enters recovery mode, remove the short-circuit between DBG_TXD and DBG_RXD.
4. Upgrade firmware via debug UART interface.

NOTE

Since the baud rate of the debug UART interface required to download firmware to the baseband chip is 3 Mbps, the flow control pins of the debug UART interface need to be reserved. Otherwise, you can only download with a 921600 baud rate, which is very slow. Test points must be reserved for DBG_TXD and DBG_RXD, and keep DBG_TXD close to DBG_RXD.

3.8. Power Supply

3.8.1. Power Supply Pins

The module has two VBAT pins for connection with an external power supply.

The following table shows the details of VBAT_BB and VBAT_RF pins and ground pins.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	19	Power supply for the module's baseband part	2.2	3.3	4.35	V
VBAT_RF	20	Power supply for the module's RF part	3.1	3.3	4.3	V
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89		-	-	-	-

NOTE

When the module is turned on normally, in order to ensure full functionality mode, the minimum power supply voltage should be at least 3.1 V.

3.8.2. Voltage Stability Requirements

The power supply range of VBAT_BB is 2.2–4.35 V, and that of VBAT_RF is 3.1–4.3 V. When the module is turned on normally, to ensure full functionality mode, the minimum power supply voltage should be at least 3.1 V.

To decrease voltage drop, one bypass capacitor of about 100 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be not less than 1 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to ensure power supply stability, it is suggested to use two TVS components with low leakage current and suitable reverse stand-off voltage, and also it is recommended to place them as close to the VBAT pins as possible. If TVS are not added, surges on the input power supplies may cause damage to the module.

The following figure shows the star structure of the power supply.

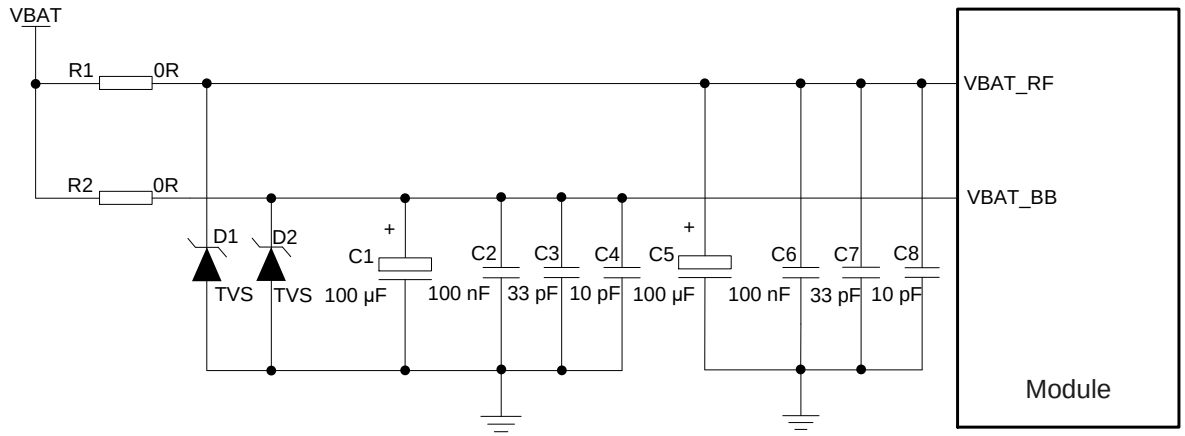


Figure 4: Star Structure of the Power Supply

Power design for a module is critical to its performance. The power supply of the module should be able to provide sufficient current of at least 0.8 A, so it is recommended to select a DC-DC converter chip or

an LDO chip with ultra-low leakage current and current output not less than 1.0 A for the power supply design.

3.8.3. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT voltage value. For more details, see ***document [3]***.

3.9. Turn On and Off Scenarios

3.9.1. Turn On with PWRKEY

The following table shows the pin description of PWRKEY.

Table 10: Pin Desciption of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	46	DI	Turn on/off the module	Internally pulled up. A test point is recommended to be reserved.

When the module is in turn-off mode, driving PWRKEY low for 500–1000 ms and then releasing it will turn on the module. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference design is illustrated in the following figure.

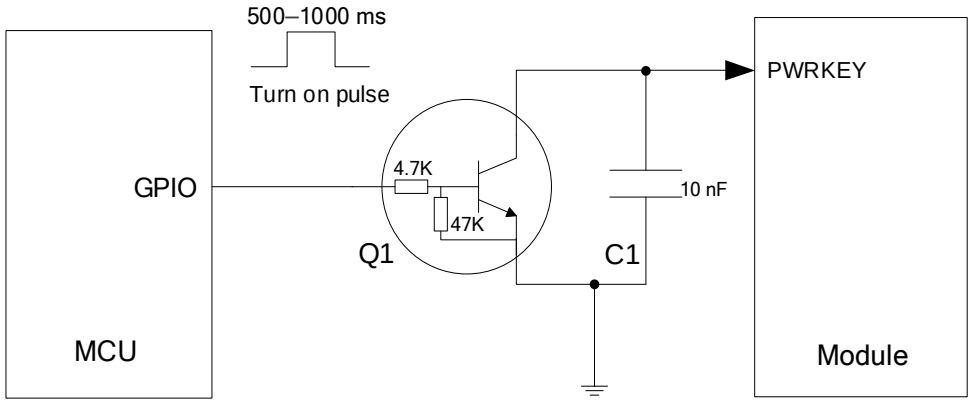


Figure 5: Turn On the Module with Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from fingers. Therefore, a TVS component is indispensable to be

placed nearby the button for ESD protection. A reference design is shown in the following figure.

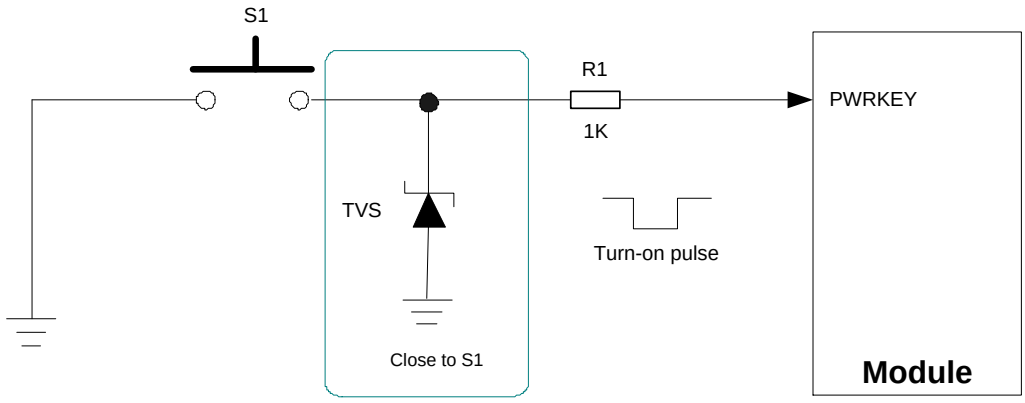


Figure 6: Turn On the Module with a Button

3.9.1.1. Power-up Timing for the Module

After the module is turned off with the PWRKEY solution (see ***Chapter 3.9.2.1***) or the AT command solution (see ***Chapter 3.9.2.2***), VBAT will keep powered on all the time until the main power supply is disconnected. In this case, driving PWRKEY low will power-up the module, and the power-up timing is shown below.

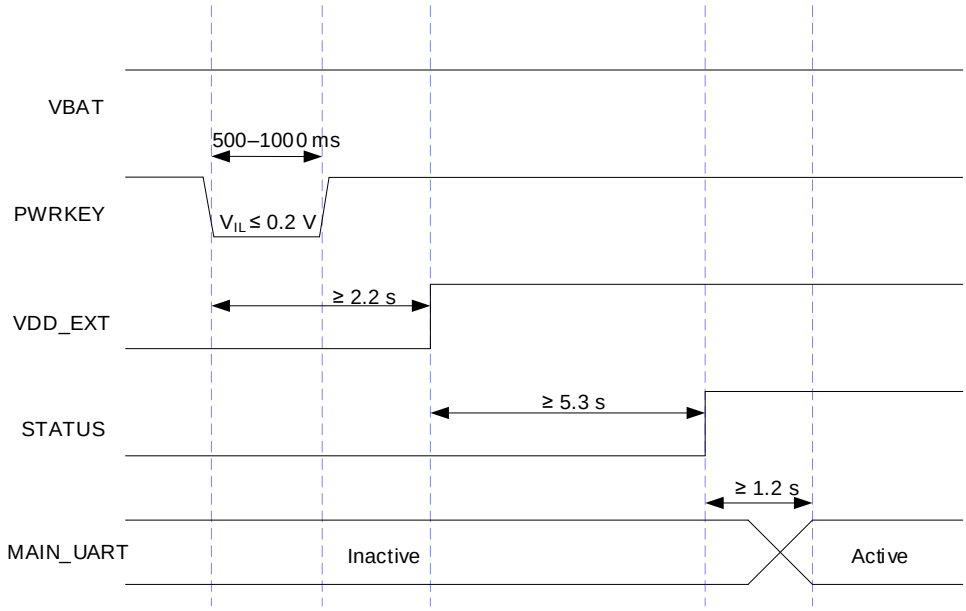


Figure 7: Power-up Timing after Power Down (PWRKEY)

NOTE

The duration of the low level of the PWRKEY should be controlled between 256 ms and 2 s.

3.9.2. Turn Off

After the module is turned off or enters PSM, do not pull up any I/O pin lest it cause additional power consumption and possibly damage pins on the module.

Either of the following methods can be used to turn off the module normally:

- Turn off the module with PWRKEY.
- Turn off the module with **AT+QPOWD**. See ***document [3]*** for more details about AT command.

3.9.2.1. Turn Off with PWRKEY

Drive PWRKEY low for 650–1500 ms before you release it. Afterwards, the module will execute a power-down procedure.

The power-down timing is illustrated in the following figure.

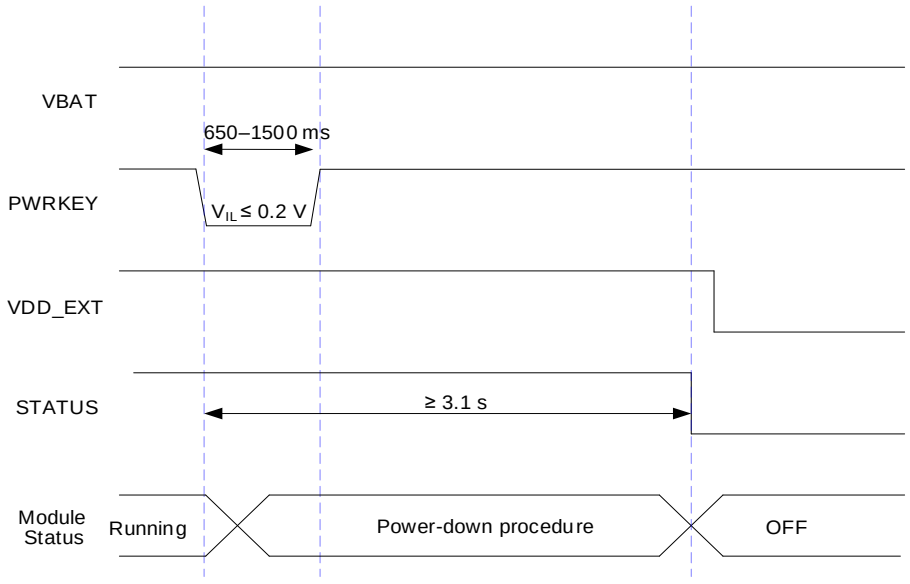


Figure 8: Power-down Timing (PWRKEY)

3.9.2.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

For details about **AT+QPOWD**, please see ***document [3]***.

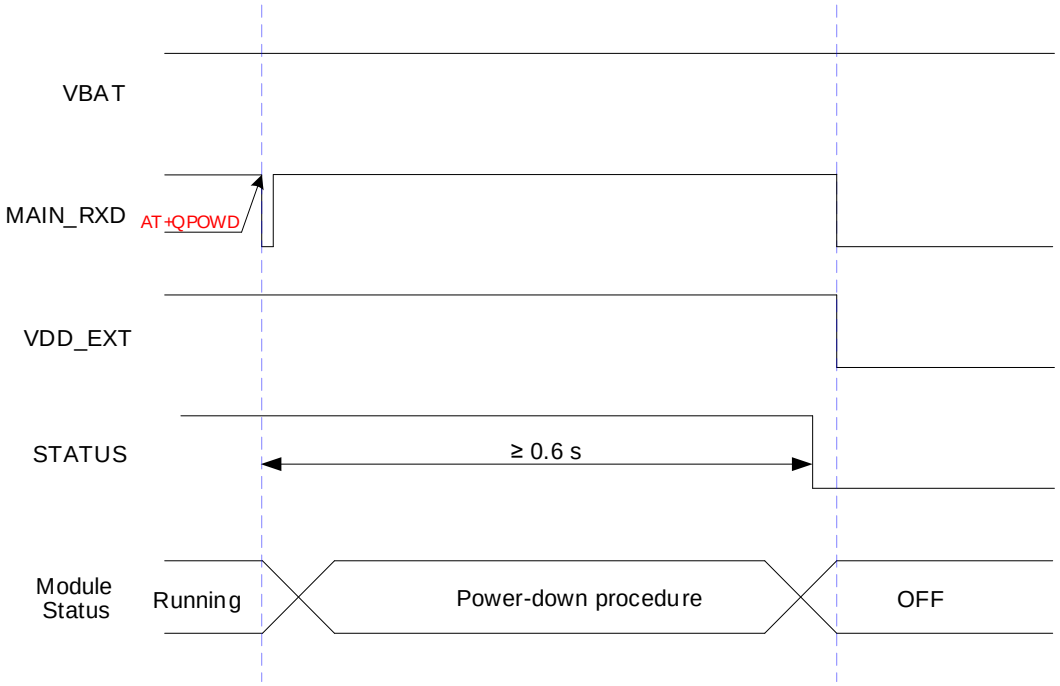


Figure 9: Power-down Timing (AT Command)

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY or AT command.
2. When turning off the module with AT command, keep PWRKEY at high level after executing turn-off command. Otherwise, the module will be turned on again after turned off.

3.10. Reset

The module can be reset by driving RESET_N low for at least 100 ms and then releasing it.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	45	DI	Reset the module.	Active low. Internally pulled up. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

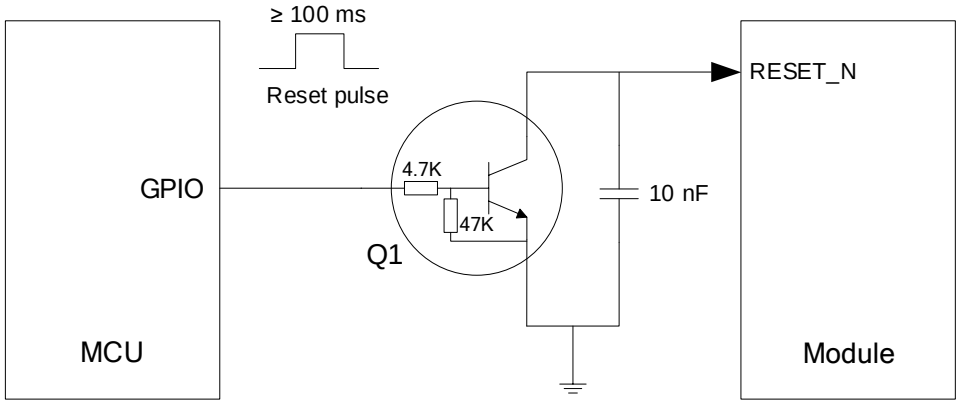


Figure 10: Reference Design of RESET_N with Driving Circuit

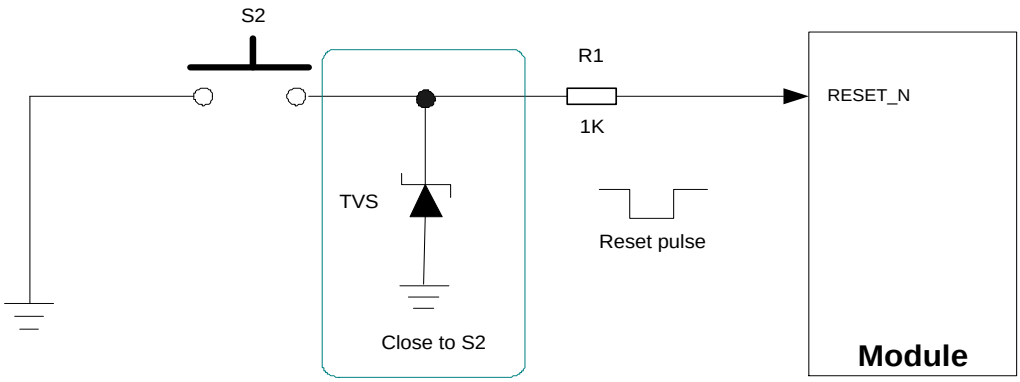


Figure 11: Reference Design of RESET_N with Button

The reset timing is illustrated in the following figure.

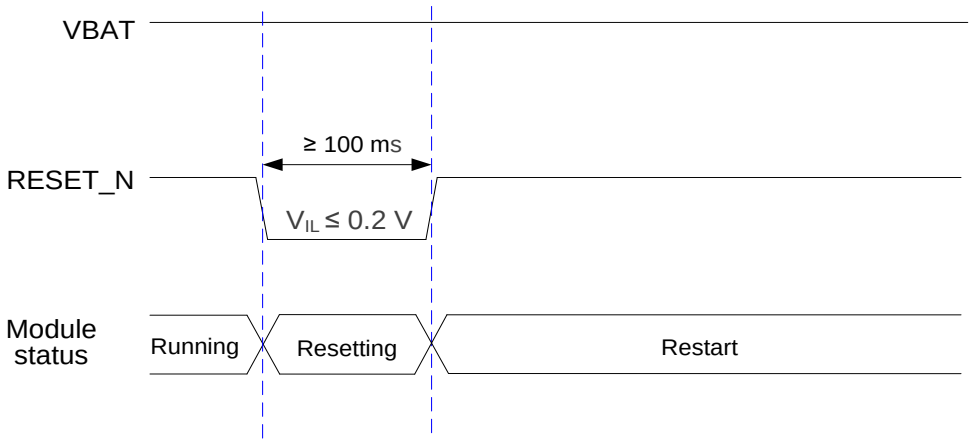


Figure 12: Reset Timing

NOTE

1. Ensure that there is no large capacitance on RESET_N pin.
2. Because PWRKEY and RESET_N traces are sensitive signal traces, it's necessary to surround the traces with ground on that layer and with ground planes above and below, and keep their traces away from each other, so as to reduce interference.

3.11. PON_TRIG

The module features one PON_TRIG pin. PON_TRIG is pulled down by default.

After sending **AT+QPSMS** to enable PSM, driving PON_TRIG low will set the module to PSM. Drive PON_TRIG high and keep it high, the module will wake up from PSM. See ***document [3]*** for more details about AT commands.

Table 12: Pin Description of PON_TRIG

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	72	DI	Wake up the module from PSM.	Internally pulled down by default. If unused, keep this pin open. A test point is recommended to be reserved.

PON_TRIG must be designed to allow for external control. A reference design is shown in the following figure.

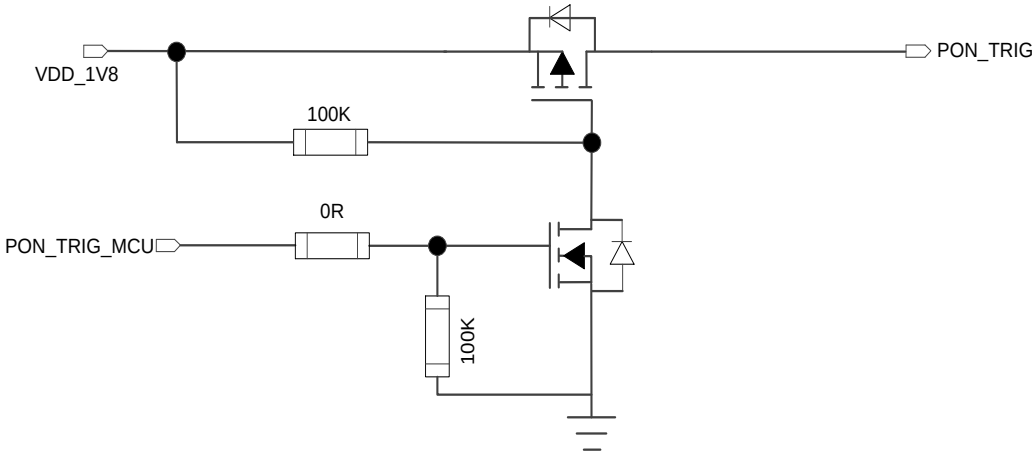


Figure 13: PON_TRIG Reference Circuit 1

In addition, a voltage divider circuit can be used to control PON_TRIG. The voltage domain of the external MCU and the voltage divider resistor should be selected with care. A voltage divider circuit in the 3.3 V MCU voltage domain is shown in the following figure.

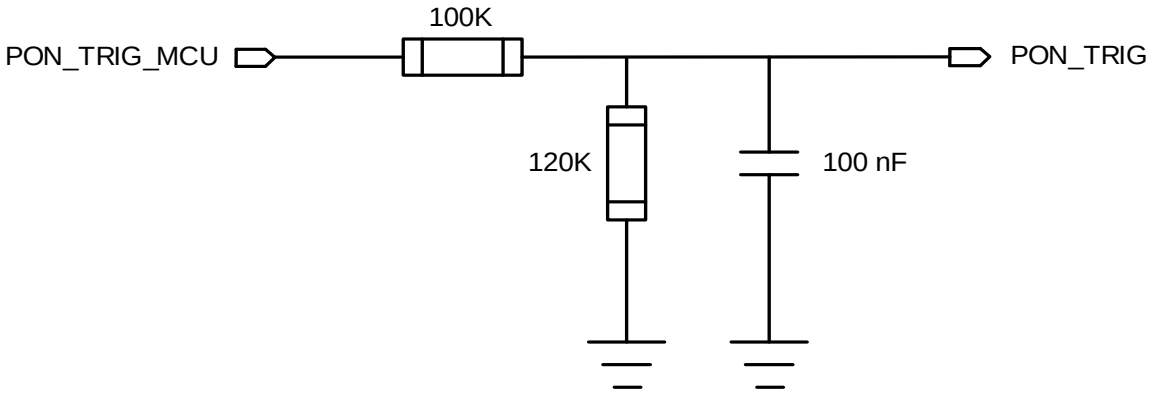


Figure 14: PON_TRIG Reference Circuit 2

NOTE

1. VDD_1V8 is powered by an external LDO.
2. If the MCU's voltage domain is not 3.3 V, the value of the voltage divider resistors should be tested according to your actual application.
3. Inside the module, PON_TRIG is connected in parallel with a 100 kΩ pull-down resistor to the ground.

4 Application Interfaces

The module is equipped with 94 LGA pins for connection to cellular application platforms. The subsequent chapters provide detailed description of interfaces listed below:

- USIM interface
- UART interfaces
- Indication signals
- ADC interfaces
- GPIO interfaces
- PCM interfaces*
- I2C interfaces*

4.1. USIM Interface

The module supports 1.8 V USIM card only. The USIM interface circuitry meets ETSI and IMT-2000 requirements.

Table 13: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	44	DI	USIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_VDD	16	PO	USIM card power supply	Only 1.8 V USIM card is supported.
USIM_RST	15	DO	USIM card reset	1.8 V power domain.
USIM_DATA	14	DIO	USIM card data	1.8 V power domain.
USIM_CLK	13	DO	USIM card clock	1.8 V power domain.
USIM_GND	65	-	Dedicated ground for USIM card	Connect this pin to ground.

The module supports USIM card hot-plug via USIM_DET, and both high-level and low-level detections are supported. The function is disabled by default, for more details about **AT+QSIMDET**, please see ***document [3]***.

The following figure shows a reference design of USIM interface with an 8-pin USIM card connector.

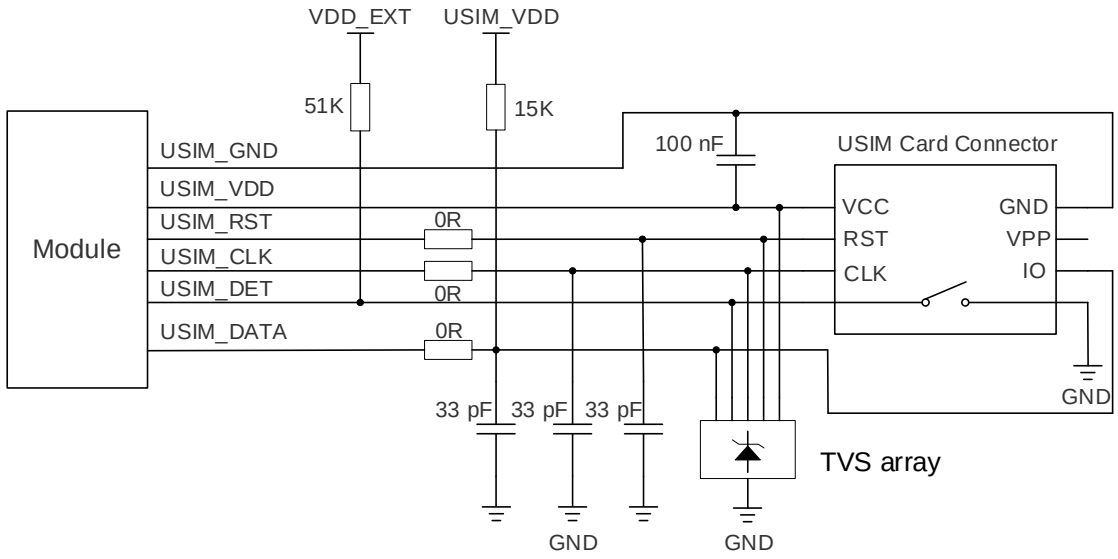


Figure 15: Reference Design of USIM Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, keep USIM_DET unconnected. A reference design for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

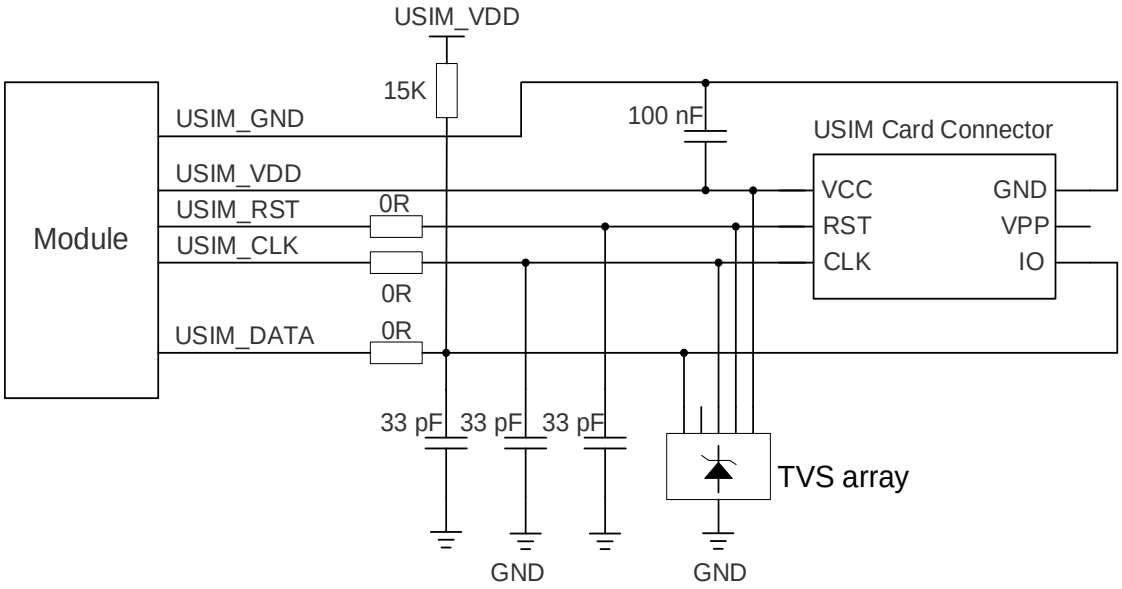


Figure 16: Reference Design of USIM Interface with a 6-Pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the criteria below in USIM circuit design:

- Place the USIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signals away from RF and VBAT traces.
- Ensure a short and wide ground trace between the module and the USIM card connector. Keep the ground and USIM_VDD traces at least 0.5 mm wide to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to USIM card connector as possible. If the system ground plane is complete, USIM_GND can be directly connected to the system ground.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep their traces away from each other and shield them with ground. USIM_RST should also be shielded with ground.
- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 15 pF. It is recommended to reserve 0 Ω series resistors for the USIM signals of the module to facilitate debugging. The 33 pF capacitors are used for filtering RF interference. Note that the USIM peripheral circuit should be close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability, and should be placed close to the USIM card connector.

4.2. UART Interfaces

The module provides two UART interfaces: main UART interface and debug UART interface. Features of them are illustrated below:

- The main UART interface supports 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default is 115200 bps. It is used for data transmission and AT command communication, GNSS data and NMEA sentences output and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default is 115200 bps. It is used for firmware upgrade, software debugging, FW log output and RF calibration, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

The following tables show the pin description of two UART interfaces.

Table 14: Pin Description of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep these pins open. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
MAIN_RXD	6	DI	Main UART receive	
MAIN_TXD	7	DO	Main UART transmit	
MAIN_CTS	39	DO	Clear to send signal from the module	
MAIN_RTS	38	DI	Request to send signal to the module	
MAIN_DCD	90	DO	Main UART data carrier detect	
MAIN_RI	76	DO	Main UART ring indication	

NOTE

AT+IPR can be used to set the baud rate of the main UART interface, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). For more details about these AT commands, please see ***document [3]***.

Table 15: Pin Description of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	60	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
DBG_RXD	61	DI	Debug UART receive	
DBG_CTS	51	DO	Clear to send signal from the module	
DBG_RTS	92	DI	Request to send signal to the module	

The module features 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. It is recommended to use a level-shifting chip without internal pull-up. The voltage-level translator TXB0108PWR provided by Texas Instruments is recommended. The following figure shows a reference design of the main UART interface:

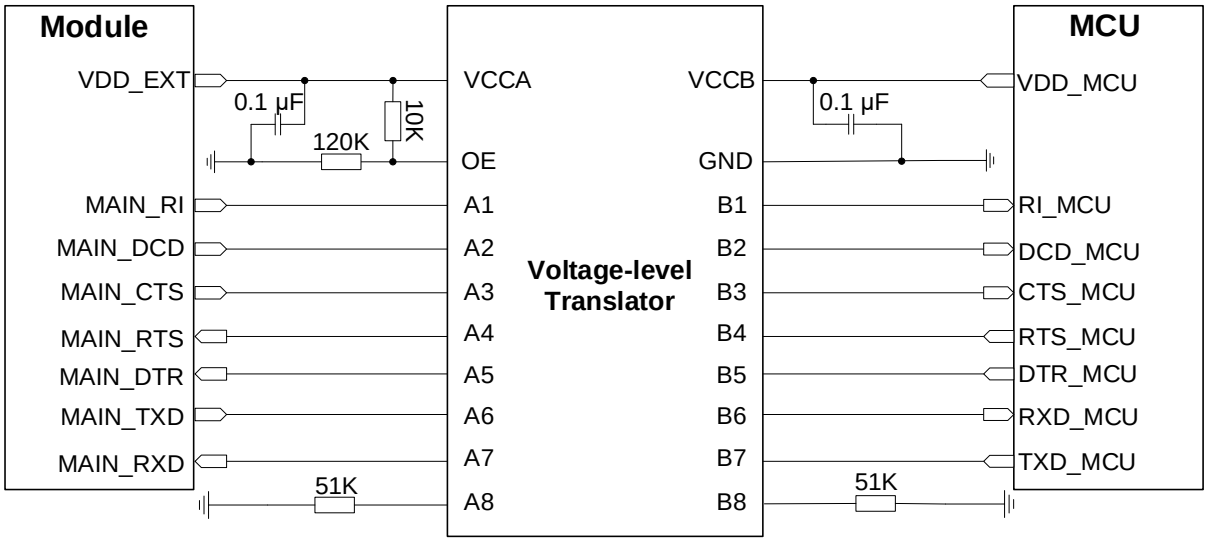


Figure 17: Main UART Reference Design (IC Solution)

Visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

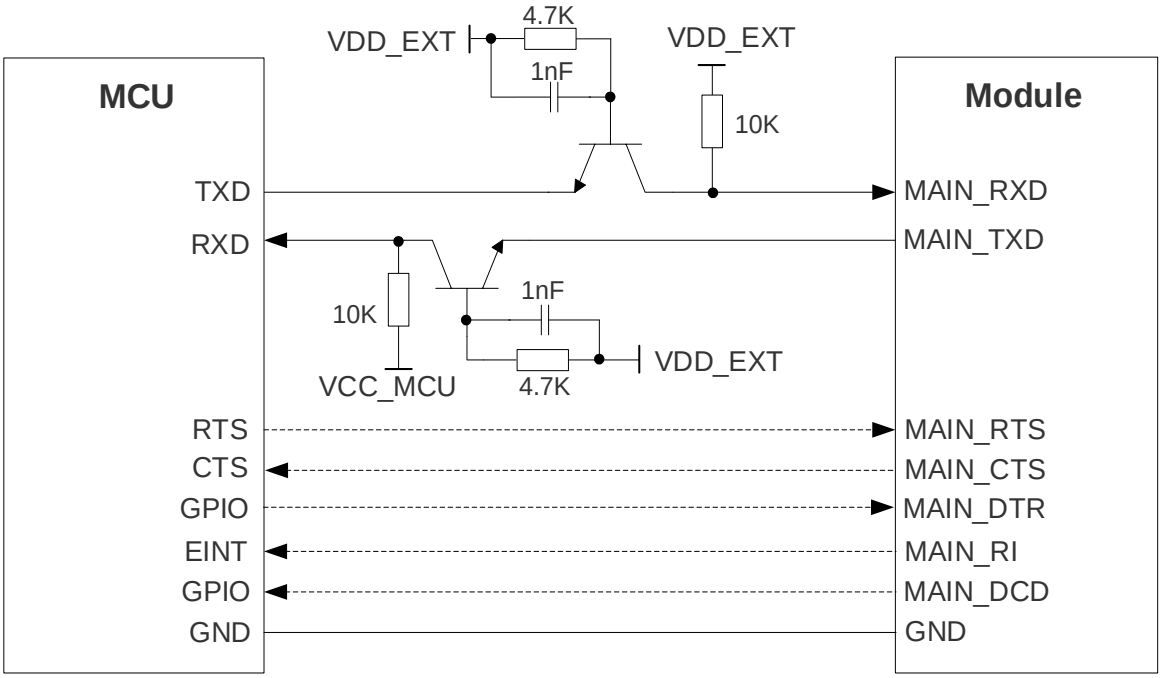


Figure 18: Main UART Reference Design (Transistor Solution)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. The main UART interface should be disconnected in PSM and turn-off modes lest it cause additional power consumption and potentially damage pins on the module.
3. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
4. The level-shifting circuits (***Figure 17*** and ***Figure 18***) use the main UART as an example. The circuits of the debug UART are connected in the same way as the main UART.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.3. Indication Signals

4.3.1. Network Status Indication

The module features one network status indication pin: NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin description and logic level changes of NET_STATUS in different network activity status.

Table 16: Pin Description of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	79	DO	Indicate the module's network activity status	1.8 V power domain. If this pin is unused, keep it open.

Table 17: Working State of NET_STATUS

Pin Name	Logic Level Change	Working Status
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Ongoing data transmission

A reference design is shown in the following figure.

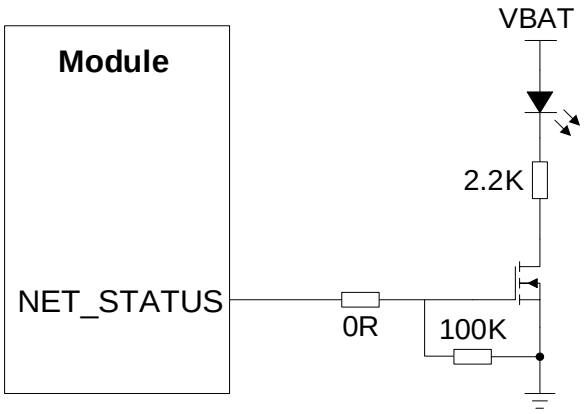


Figure 19: Reference Design of NET_STATUS

4.3.2. STATUS

The STATUS pin indicates the operation status of the module. It outputs high level when the module turns on.

Table 18: Pin Description of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	78	DO	Indicate the module's operation status	1.8 V power domain. If the pin is unused, keep it open.

The following figure shows a reference design of STATUS.

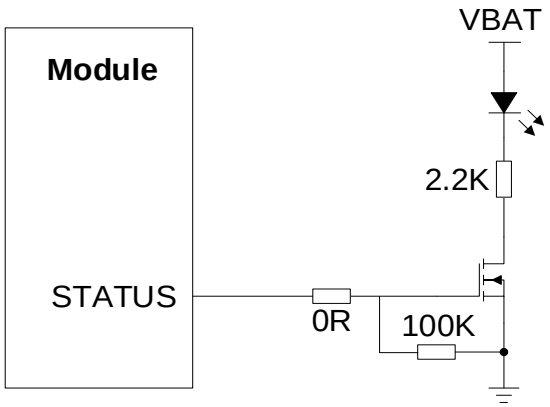


Figure 20: Reference Design of STATUS

4.3.3. MAIN_RI

Table 19: Pin Description of MAIN_RI

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	76	DO	Main UART ring indication	1.8 V power domain. If the pin is unused, keep it open

The default behaviors of MAIN_RI are shown as below.

Table 20: Default Behaviors of MAIN_RI

Pin State	Response
Idle	MAIN_RI remains at high level.
URC	MAIN_RI outputs a 120 ms low pulse when a new URC is returned.

The default MAIN_RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/other"** and **AT+QCFG="urc/ri/smsincoming"**. For more details about **AT+QCFG**, please see ***document [5]***.

NOTE

A URC can be outputted from the main UART (default) through configuring URC indication option with **AT+QURCCFG**. For details about the AT command, please see ***document [3]***.

4.4. ADC Interfaces

The module has two Analog-to-Digital Converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0. **AT+QADC=1** can be used to read the voltage value on ADC1. For more details about the AT command, please see ***document [3]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 21: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description
ADC0	17	AI	General-purpose ADC interface
ADC1	18	AI	General-purpose ADC interface

The following table describes the characteristics of ADC interfaces.

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Input Voltage Range	0	-	1.8	V
Resolution	6	-	12	bit

NOTE

1. It is prohibited to directly supply any voltage to the ADC interface before the module is powered up.
2. It is recommended to use resistor divider circuit for ADC application, and the divider's resistor accuracy should be at least 1 %.
3. After the module is turned off or enters PSM, do not pull up any pin of ADC interfaces lest it cause additional power consumption and potentially damage pins on the module.

4.5. GPIO Interfaces

The module has thirteen general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** command can be used to configure the status of GPIO pins. For more details about the command, please see ***document [5]***.

Table 23: Pin Description of GPIO Interfaces

Pin Name	Pin No.	I/O	Description
GPIO1	1	DIO	General-purpose input/output
GPIO2	8	DIO	General-purpose input/output

GPIO3	9	DIO	General-purpose input/output
GPIO4	33	DIO	General-purpose input/output
GPIO5	40	DIO	General-purpose input/output
GPIO6	57	DIO	General-purpose input/output
GPIO7	63	DIO	General-purpose input/output
GPIO8	64	DIO	General-purpose input/output
GPIO9	67	DIO	General-purpose input/output
GPIO10	68	DIO	General-purpose input/output
GPIO11	80	DIO	General-purpose input/output
GPIO12	81	DIO	General-purpose input/output
GPIO13	91	DIO	General-purpose input/output

4.6. PCM and I2C Interfaces*

The module provides one Pulse Code Modulation (PCM) digital interface and one inter-integrated circuit (I2C) interface which are used for VoLTE.

The following table shows the pin description of the two interfaces which can be applied to audio codec design.

Table 24: Pin Description of PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	35	DIO	PCM data frame sync	In master mode, they are output signals. In slave mode, they are input signals. If unused, keep these pins open.
PCM_CLK	3	DIO	PCM clock	
PCM_DIN	2	DI	PCM data input	If unused, keep these pins open.
PCM_DOUT	34	DO	PCM data output	

Table 25: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	37	OD	I2C serial clock	1.8 V only. External pull-up resistors are required. If unused, keep these pins open.
I2C_SDA	5	OD	I2C serial data	

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

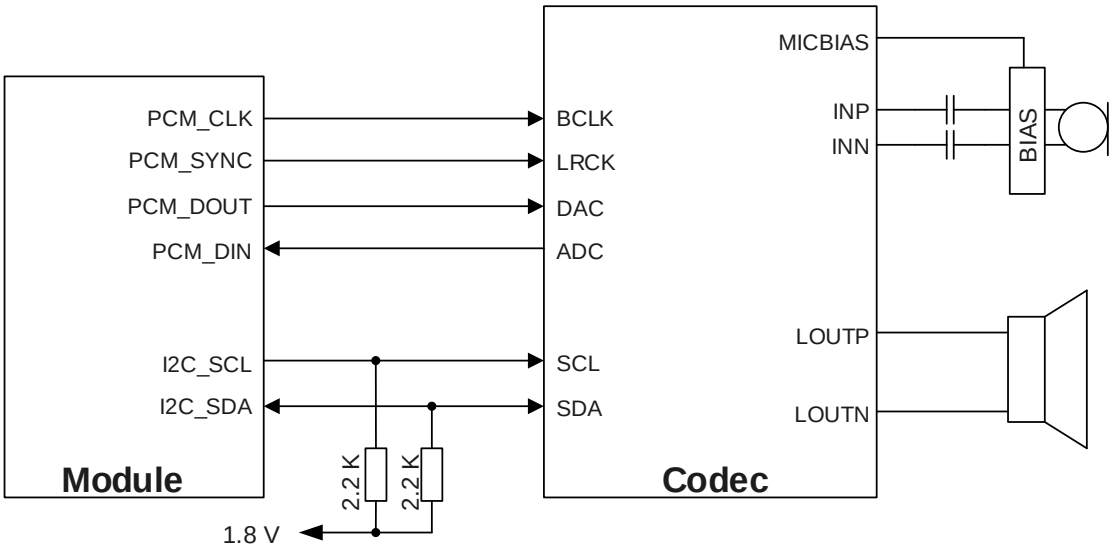


Figure 21: Reference Design of PCM and I2C Interfaces

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module includes a main antenna interface and a GNSS antenna interface. The impedance of antenna interfaces is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Description

The pin description of the main antenna interface is shown below.

Table 26: Pin Description of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	26	AIO	Main antenna interface	50 Ω impedance.

5.1.2. Operating Frequency

Table 27: BG770S-GL Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE HD-FDD B2	1850–1910	1930–1990	MHz
LTE HD-FDD B3	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz

LTE HD-FDD B5	824–849	869–894	MHz
LTE HD-FDD B8	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz
LTE HD-FDD B13	777–787	746–756	MHz
LTE HD-FDD B17 [6]	704–716	734–746	MHz
LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26 [7]	814–849	859–894	MHz
LTE HD-FDD B27 [8]	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz
LTE HD-FDD B85	698–716	728–746	MHz

5.1.3. Antenna Tuner Control Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 28: Pin Description of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comments
GRFC1	83	DO	Generic RF controller	1.8 V power domain. If these pins are unused, keep them open. Test points are recommended to be reserved.
GRFC2	94	DO	Generic RF controller	

[6] LTE HD-FDD B17 is supported in Cat NB2 only.
[7] LTE HD-FDD B26 is supported in Cat M1 and NB2.

Table 29: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)
Low	Low	880–2180
Low	High	791–879.9
High	Low	698–790.9

5.1.4. Transmit Power

Table 30: Transmit Power

Frequency Bands	Max. Transmit Power	Min. Transmit Power
LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17 [6]/B18/ B19/B20/B25/B26 [7]/B27 [8]/B28/B66/B85	23 dBm ±2 dB	< -39 dBm

5.1.5. Receiver Sensitivity

Table 31: Conducted RF Receiving Sensitivity

Frequency Band	Primary Cat M1	Primary Cat NB2	Receiving Sensitivity (dBm)	
			Cat M1/3GPP	Cat NB2 [9] /3GPP
LTE HD-FDD B1	-106.2	-112.9	-102.3	-107.5
LTE HD-FDD B2	-106.2	-114.2	-100.3	-107.5
LTE HD-FDD B3	-106.2	-114.2	-99.3	-107.5
LTE HD-FDD B4	-106.2	-114.2	-102.2	-107.5
LTE HD-FDD B5	-106.2	-114.2	-100.8	-107.5
LTE HD-FDD B8	-106.2	-114.2	-99.8	-107.5
LTE HD-FDD B12	-106.2	-114.2	-99.3	-107.5

[8] LTE HD-FDD B27 is supported in Cat M1 only.
[9] LTE Cat NB is single-transmission receiving sensitivity.

LTE HD-FDD B13	-106.2	-114.2	-99.3	-107.5
LTE HD-FDD B17 [6]	-	-114.2	-	-107.5
LTE HD-FDD B18	-106.2	-114.2	-102.3	-107.5
LTE HD-FDD B19	-106.2	-114.2	-102.3	-107.5
LTE HD-FDD B20	-106.2	-114.2	-99.8	-107.5
LTE HD-FDD B25	-106.2	-114.5	-100.3	-107.5
LTE HD-FDD B26 [7]	-106.2	-114.2	-100.3	-107.5
LTE HD-FDD B27 [8]	-106.2	-	-100.8	-
LTE HD-FDD B28	-106.2	-114.2	-100.8	-107.5
LTE HD-FDD B66	-106.2	-114.2	-101.8	-107.5
LTE HD-FDD B85	-106.2	-114.2	-99.3	-107.5

5.1.6. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a dual L-type circuit for better RF performance, and the dual L-type components (R1/C1/C2/C3) should be placed as close to the antenna as possible. The capacitors C1 and C2 are not mounted by default.

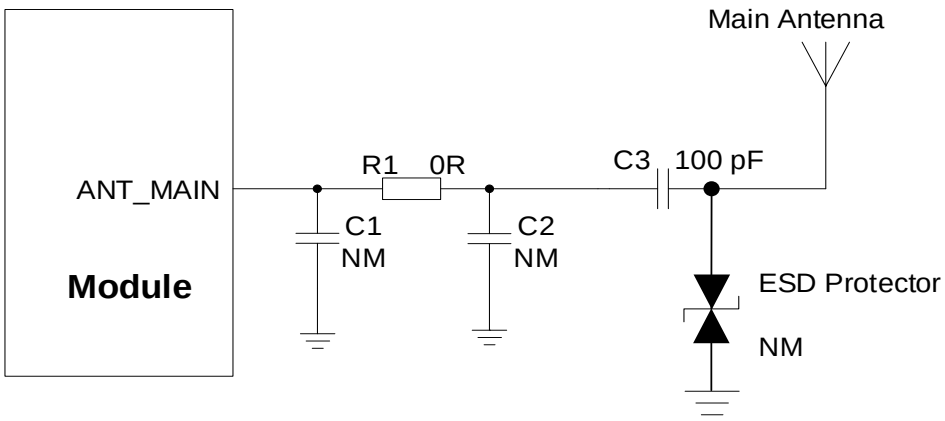


Figure 22: Reference Design of Main Antenna Interface

NOTE

1. It is recommended to reserve ESD protection component for the antenna interface to effectively prevent static electricity and the junction capacitance should not exceed 0.05 pF.
2. Notes on C3:
   1) If there is DC power at the antenna ports, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C3.
      b) If C3 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor. You can also match the component according to the debugging results.

5.2. GNSS Antenna Interface

5.2.1. General Description

The module supports GPS and GLONASS* satellite systems using dedicated hardware accelerators in a power and cost-efficient manner.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via main UART interface by default.

By default, the module's GNSS engine is switched off. It has to be switched on via **AT+QGPS**. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [6]***.

5.2.2. Pin Description

Table 32: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	32	AI	GNSS antenna interface	50 Ω impedance. If this pin is unused, keep it open.

5.2.3. GNSS Operating Frequency

Table 33: GNSS Operating Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023 (L1)	MHz
GLONASS*	1601.7 ±4.2 (L1)	MHz

5.2.4. GNSS Performance

The following table shows the GNSS performance of the module.

Table 34: GNSS Performance

Parameter	Specification	BG770S-GL
Default Constellation	-	GPS, GLONASS*
Power Consumption [10] Combo Mode [11]	Acquisition	30.03 mA
	Tracking	9.67 mA
Sensitivity	Acquisition	-148 dBm
	Reacquisition	-156 dBm
	Tracking	-160 dBm
TTFF [10] (Without AGNSS)	Cold Start	32.38 s
	Warm Start	30.27 s
	Hot Start	0.08 s
TTFF [12] (With AGNSS)	Cold Start	14.3 s
Horizontal Position Accuracy	Autonomous [13]	L1: 0.8561 m

[10] Tested at default constellation and room temperature, with typical operating voltage, and satellite signal of -130 dBm configured by the instrument.
[11] The power consumption includes cellular power consumption, with the cellular module operating under **AT+CFUN=0**.
[12] Open-sky, active high precision GNSS antenna.
[13] CEP 50 %, open-sky 12 hours static, more than 8 SVs.

Vertical Accuracy		0.5 m
Update Rate	PVT [14]: 1 Hz (Max.)	
Velocity Accuracy [10]	0.1 m/s	
Dynamic Performance [15]	Maximum Altitude: 10000 m Maximum Velocity [16]: 500 m/s Maximum Acceleration [16]: 1 g	

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.5. Reference Design

A reference design of GNSS antenna interface is shown as below.

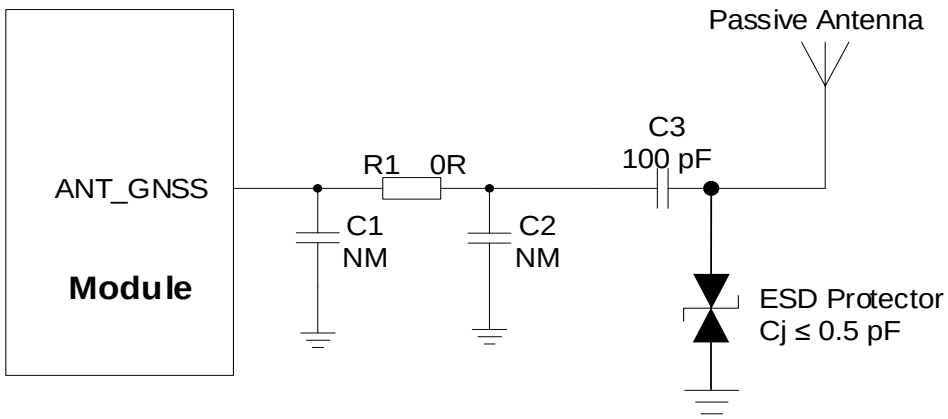


Figure 23: Reference Design of GNSS Antenna Interface

[14] PVT: Position, Velocity and Time.
[15] Tested at default constellation and room temperature, with typical operating voltage, and satellite signal of -130 dBm.
[16] ITAR limit.

NOTE

1. The module is designed with a built-in LNA, and supports passive GNSS antenna only. Active antenna and external LNA are not supported.
2. Notes on C3:
   1) If there is DC power at the antenna ports, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C3.
      b) If C3 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor. You can also match the component according to the debugging results.

5.3. RF Routing Guidelines

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

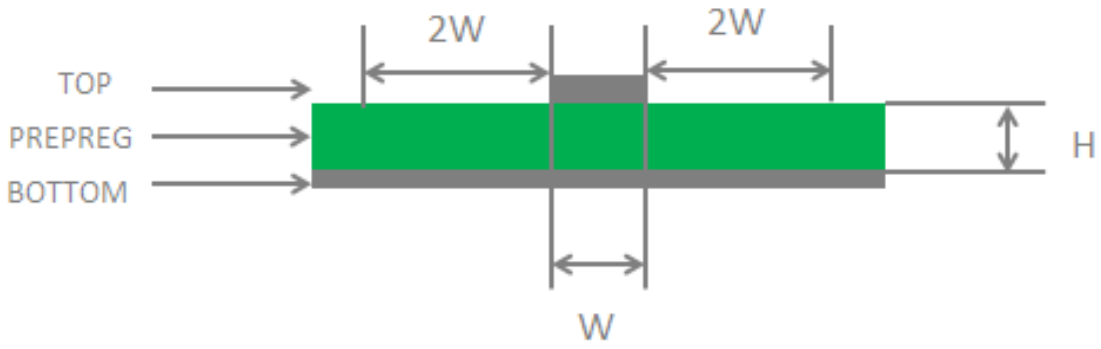


Figure 24: Microstrip Design on a 2-layer PCB

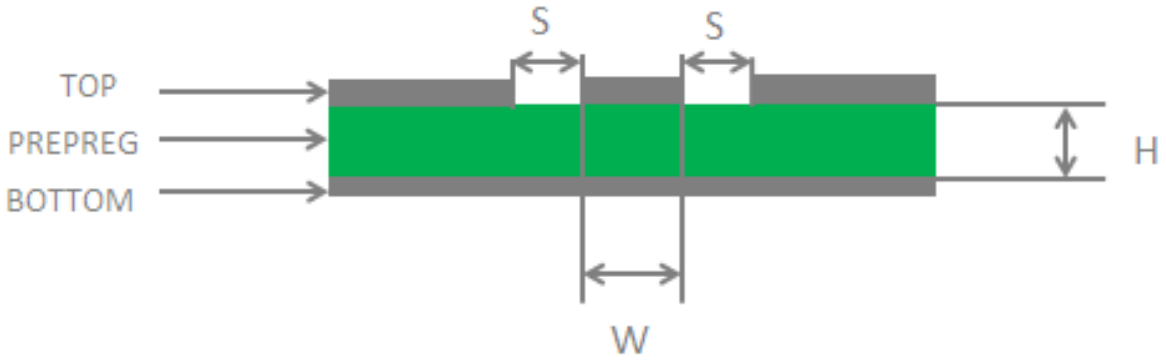


Figure 25: Coplanar Waveguide Design on a 2-layer PCB

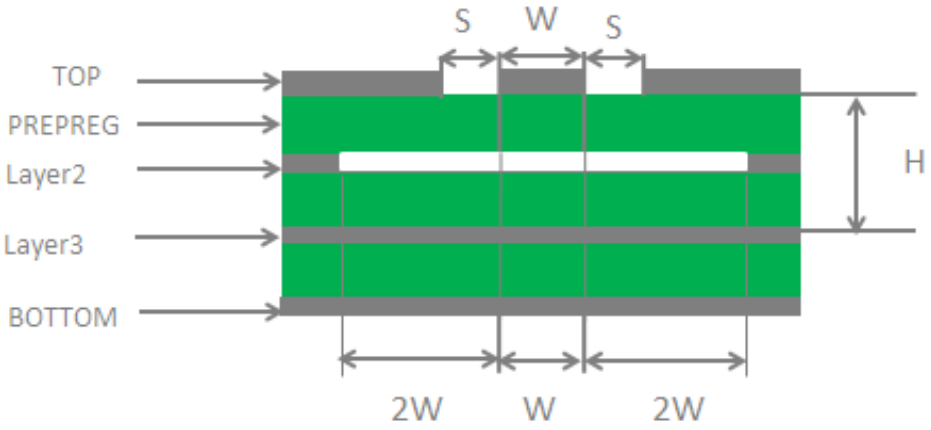


Figure 26: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

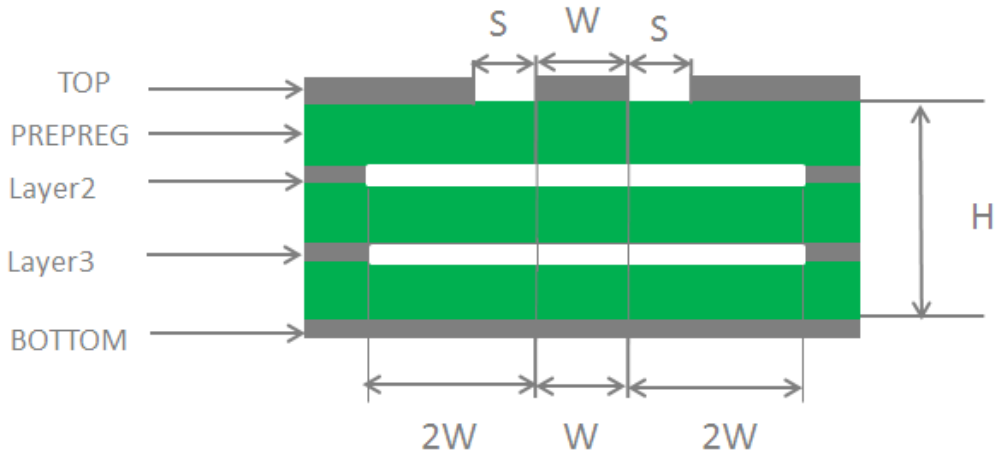


Figure 27: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [7]***.

5.4. Requirements for Antenna Design

5.4.1. Antenna Design Requirements

The following table shows the requirements on the main antenna and the GNSS antenna.

Table 35: Antenna Design Requirements

Antenna Type	Requirements
GNSS	Must be a passive antenna Frequency range: 1559–1606 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.) Passive antenna gain: > 0 dBi
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

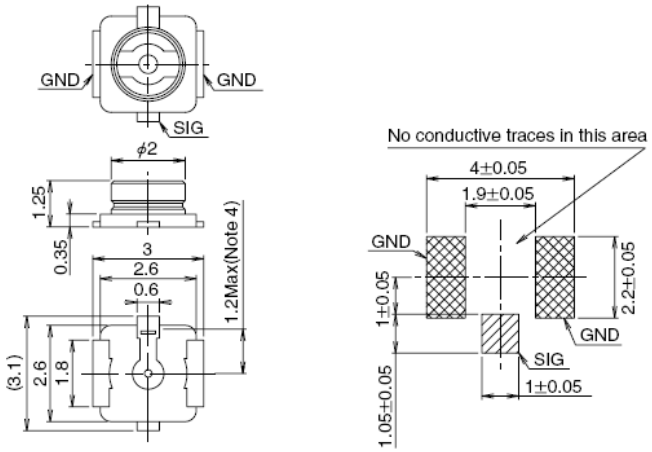


Figure 28: Dimensions of the Receptacle (Unit: mm)

The mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

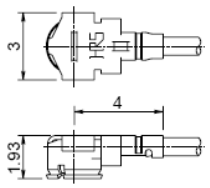
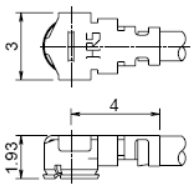
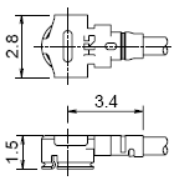
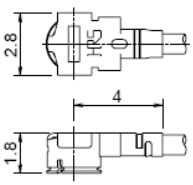
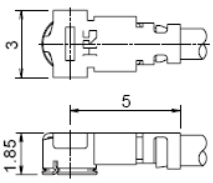
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 29: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

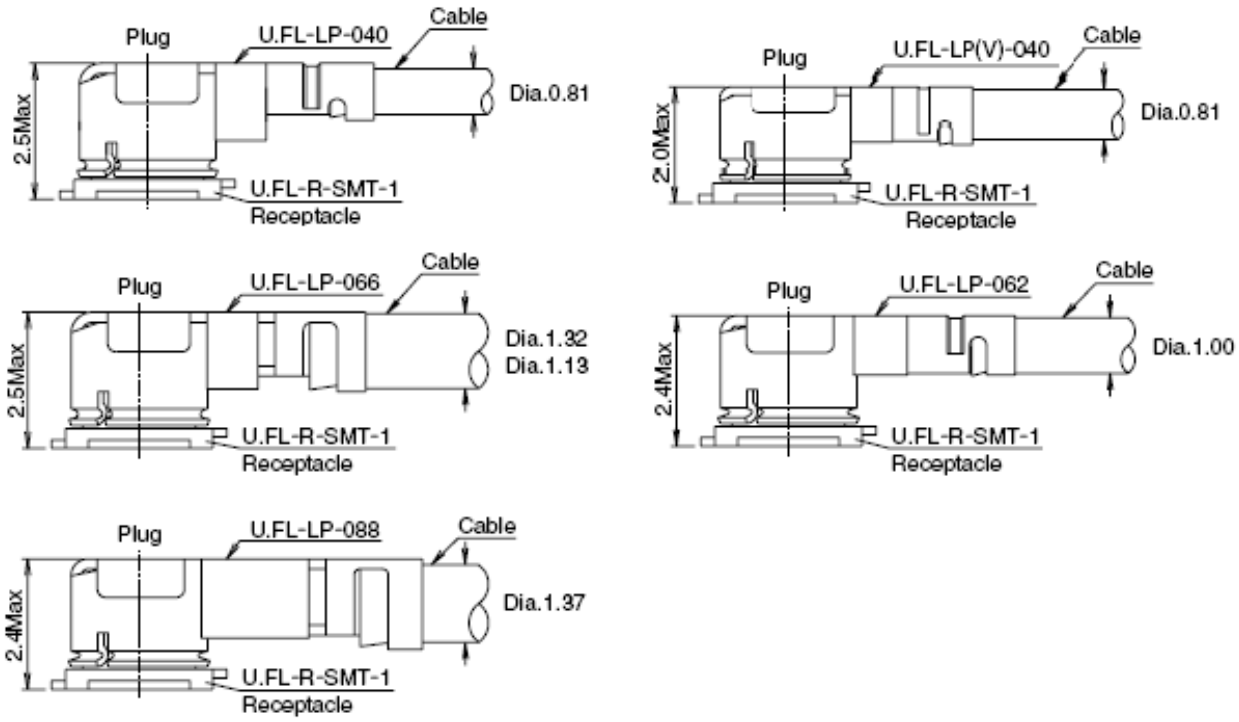


Figure 30: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.2	4.5	V
VBAT_RF	-0.2	4.5	V
Voltage at Digital Pins	-0.2	1.98	V

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

6.2. Power Supply Ratings

Table 37: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB [17]	Power supply for the module's baseband part	The actual input voltages must be kept between the minimum and maximum values.	2.2	3.3	4.35	V
VBAT_RF [17]	Power supply for the module's RF part		3.1	3.3	4.3	V

6.3. Operating and Storage Temperatures

Table 38: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Normal Operating Temperature [18]	-35	+25	+75	ºC
Extended Operating Temperature [19]	-40	-	+85	ºC
Storage Temperature	-40	-	+90	ºC

[17] When the module is turned on normally, to ensure full functionality mode, the minimum power supply voltage should be at least 3.1 V.
[18] Within the operating temperature range, the module's indicators comply with 3GPP specification requirements.
[19] Within the range of -40 to -35 °C or 75 to 85 °C, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

6.4. Power Consumption

The following table shows the power consumption of the module.

Table 39: BG770S-GL Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Condition	Avg.	Unit
Leakage	Turn-off @ UART disconnected	1.34	μA
PSM	PSM @ UART disconnected	1.31	μA
Rock Bottom	**AT+CFUN=0** @ Sleep mode (**AT+QSCLK=2**)	4.8	μA
	AT+CFUN=0 @ Sleep mode (**AT+QSCLK=3**)	1.9	μA
Sleep Mode (**AT+QSCLK=2**) (UART disconnected)	LTE Cat M1 DRX = 1.28 s	0.315	mA
	LTE Cat NB1 DRX = 1.28 s	0.547	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 1.28 s, DRX = 1.28 s	15.064	μA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	22.043	μA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	10.002	μA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	13.034	μA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	34.826	μA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	18.262	μA
Sleep Mode (**AT+QSCLK=3**) (UART disconnected)	LTE Cat M1 DRX = 1.28 s	0.306	mA
	LTE Cat NB1 DRX = 1.28 s	0.551	mA
	LTE Cat M1 e-I-DRX = 40.96 s	12.019	μA

	@ PTW = 1.28 s, DRX = 1.28 s		
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	18.412	μA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	7.129	μA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	10.34	μA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	32.644	μA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	17.306	μA
Idle State (UART disconnected)	LTE Cat M1 DRX = 1.28 s	9.55	mA
	LTE Cat NB1 DRX = 1.28 s	9.73	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	9.31	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	9.66	mA
LTE Cat M1 data transmission (GNSS OFF)	LTE HD-FDD B1 @ 23.18 dBm	151.33	mA
	LTE HD-FDD B2 @ 23.32 dBm	149.69	mA
	LTE HD-FDD B3 @ 23.17 dBm	146.32	mA
	LTE HD-FDD B4 @ 23.19 dBm	147.01	mA
	LTE HD-FDD B5 @ 23.09 dBm	142.28	mA
	LTE HD-FDD B8 @ 23.08 dBm	145.53	mA
	LTE HD-FDD B12 @ 23.1 dBm	135.09	mA
	LTE HD-FDD B13 @ 23.1 dBm	137.847	mA
	LTE HD-FDD B18 @ 23.07 dBm	140.82	mA
	LTE HD-FDD B19 @ 23.1 dBm	141.52	mA

	LTE HD-FDD B20 @ 23.1 dBm	143.07	mA
	LTE HD-FDD B25 @ 23.31 dBm	149.83	mA
	LTE HD-FDD B26 @ 23.18 dBm	140.6	mA
	LTE HD-FDD B27 @ 23.16 dBm	140.29	mA
	LTE HD-FDD B28A @ 23.11 dBm	135.2	mA
	LTE HD-FDD B28B @ 23.16 dBm	137.04	mA
	LTE HD-FDD B66 @ 23.18 dBm	147.12	mA
	LTE HD-FDD B85 @ 23.07 dBm	134.92	mA
LTE Cat NB2 data transmission (GNSS OFF)	LTE HD-FDD B1 @ 23.17 dBm	158.68	mA
	LTE HD-FDD B2 @ 23.18 dBm	154.49	mA
	LTE HD-FDD B3 @ 23.05 dBm	150.72	mA
	LTE HD-FDD B4 @ 23.12 dBm	152.88	mA
	LTE HD-FDD B5 @ 23.98 dBm	145.39	mA
	LTE HD-FDD B8 @ 23.08 dBm	155.58	mA
	LTE HD-FDD B12 @ 22.95 dBm	137.69	mA
	LTE HD-FDD B13 @ 23.01 dBm	141.16	mA
	LTE HD-FDD B17 @ 23 dBm	137.82	mA
	LTE HD-FDD B18 @ 22.8 dBm	144.54	mA
	LTE HD-FDD B19 @ 23.03 dBm	145.93	mA
	LTE HD-FDD B20 @ 22.91 dBm	145.22	mA
	LTE HD-FDD B25 @ 23.19 dBm	154.7	mA
	LTE HD-FDD B26 @ 23.03 dBm	146.47	mA
	LTE HD-FDD B28 @ 23.03 dBm	139.37	mA
	LTE HD-FDD B66 @ 23.07 dBm	151.39	mA
	LTE HD-FDD B85 @ 22.93 dBm	137.65	mA

NOTE

The above power consumption data were obtained under a 50 Ω impedance test condition.

Table 40: BG770S-GL GNSS Power Consumption (Power Supply: 3.8 V, Room Temperature)

Description	Conditions	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Instrument	29.38	mA
	Hot start @ Instrument	30.03	mA
	Lost state @ Instrument	30.06	mA
Tracking (**AT+CFUN=0**)	Instrument environment @ Passive antenna	9.54	mA
	Half sky @ Real network, Passive antenna	9.67	mA

6.5. Digital I/O Characteristic

Table 41: VDD_EXT Digital I/O Characteristics

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.65 × VDD_EXT	1.98	V
V_{IL}	Low-level input voltage	-0.2	0.35 × VDD_EXT	V
V_{OH}	High-level output voltage	VDD_EXT - 0.4	-	V
V_{OL}	Low-level output voltage	-	0.4	V

6.6. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly, and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatic discharge characteristics of the module.

Table 42: Electrostatic Discharge Characteristics (Temperature: 15–35 °C, Humidity: 30–60 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	8	12	kV
Main Antenna Interface	5	10	kV
GNSS Antenna Interface	3	10	kV

6.7. MRAM Magnetic Field Tolerance

BG770S-GL's baseband chip includes a 4 MB MRAM (Magnetoresistive Random Access Memory), a non-volatile memory that stores data using magnetic states. The MRAM retains data without the need for a continuous power supply. MRAM is sensitive to strong magnetic fields, which can affect the behavior of the embedded MRAM (eMRAM) macro. Damage to the module can occur if it is placed in close proximity to a magnetic source. The maximum magnetic field is the maximum field strength the MRAM can tolerate without data corruption.

Table 43: Maximum Magnetic Field Specification

Parameter	Condition	Value
Maximum magnetic field	– Storage (no voltage supply) – Maximum field for 5-second exposure – At any angle, tested up to temperature of 125 °C	750 Oe (75 mT)
	– Storage (no voltage supply) – Maximum field for 10-year exposure – At any angle, tested up to temperature of 125 °C	420 Oe (42 mT)
	– Device operation – At any angle across the full temperature range	100 Oe (10 mT)

6.7.1. Precaution Guidelines

To ensure reliable performance and data integrity, and to avoid data corruption:

- Avoid placing permanent magnet or magnetic field source near to the module.
- Ensure magnetic field strength near the module does not exceed 10 mT during operation and 42 mT during storage.

- Do not operate the module near industrial magnetic equipment or high-current traces without proper shielding.
- Conduct EMI and magnetic susceptibility testing on the module to validate safe operation.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

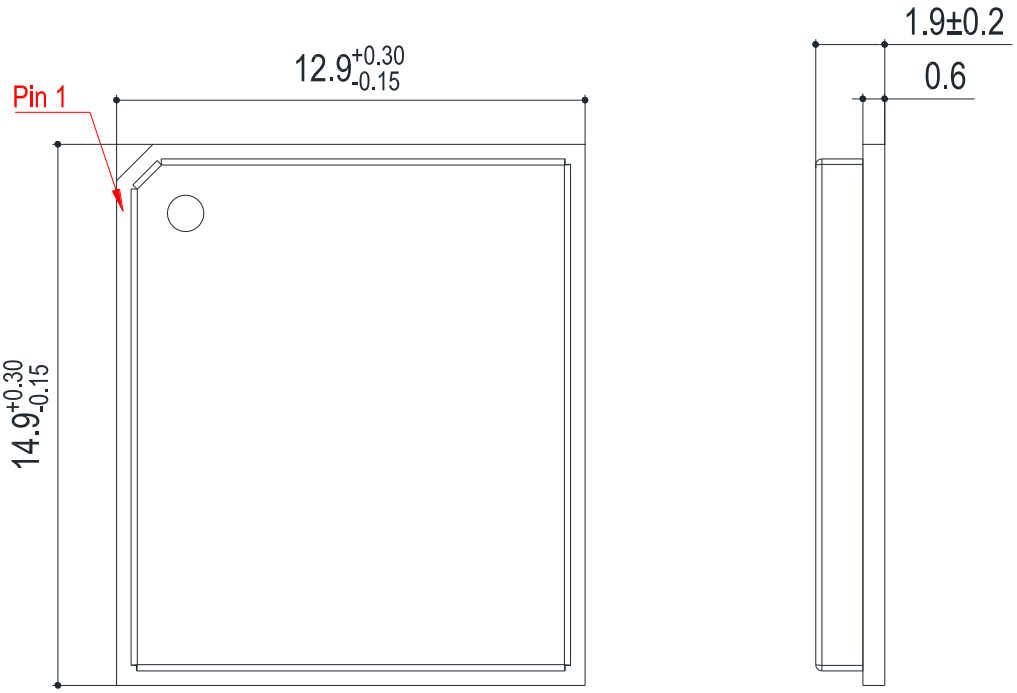


Figure 31: Module Top and Side Dimensions

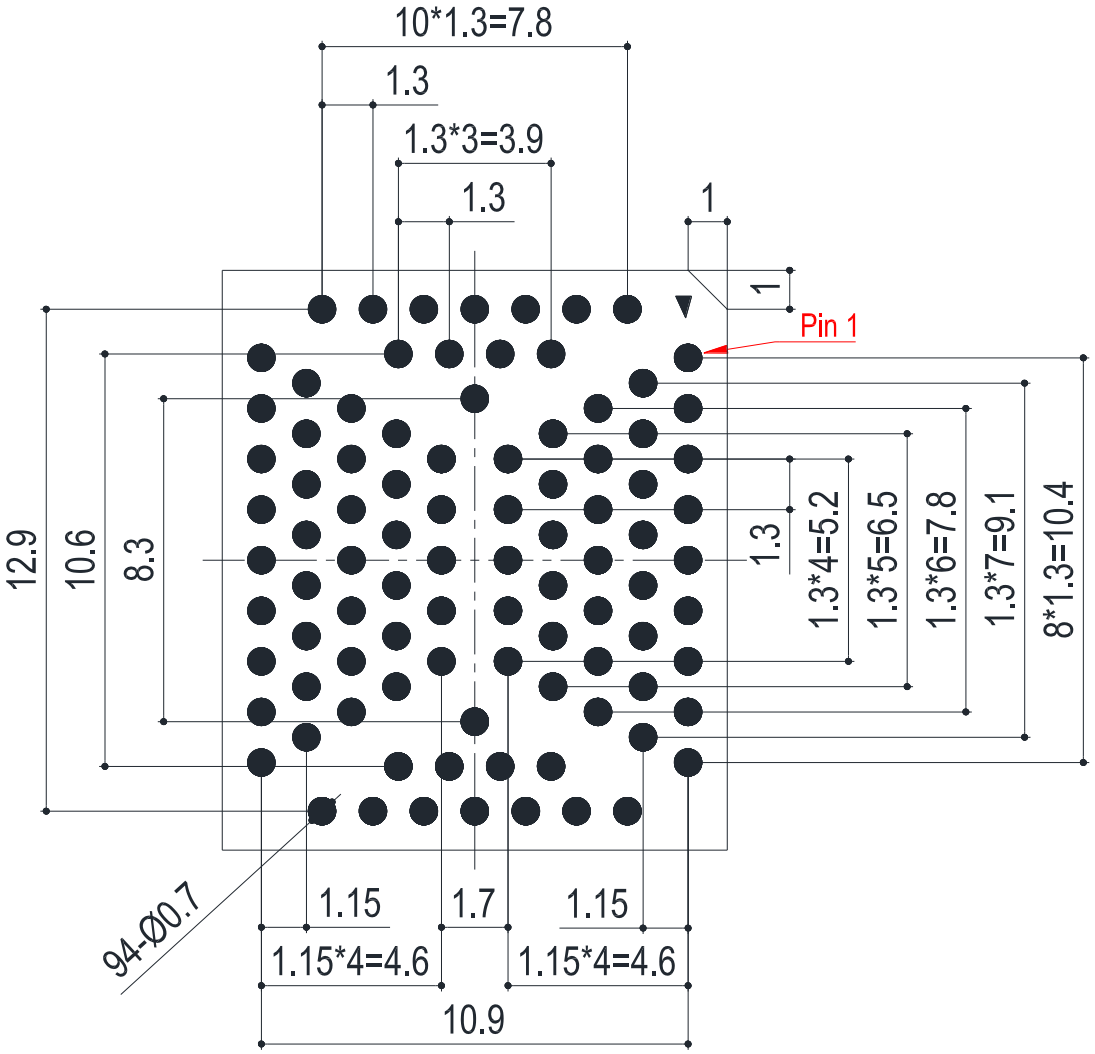


Figure 32: Bottom Dimensions (Bottom View)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

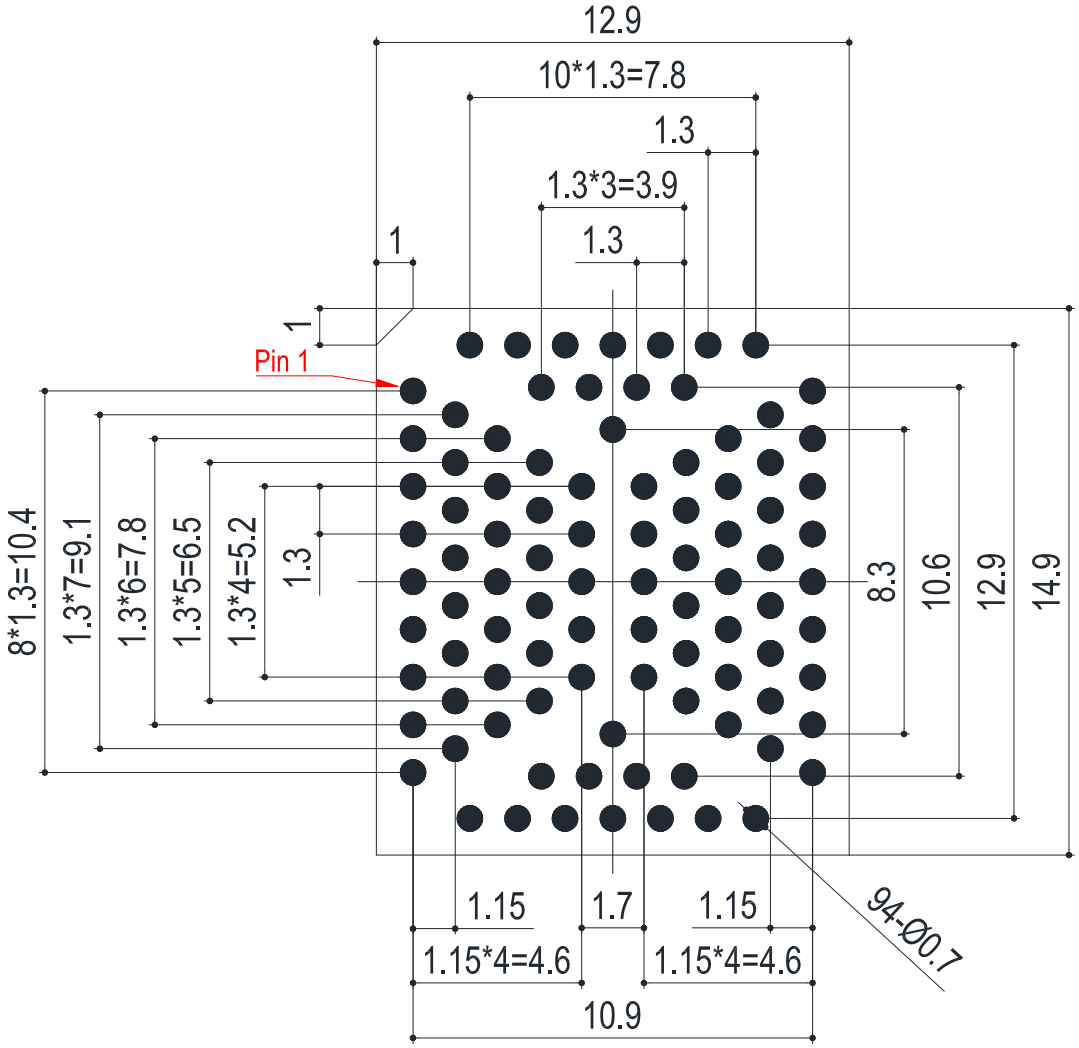


Figure 33: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

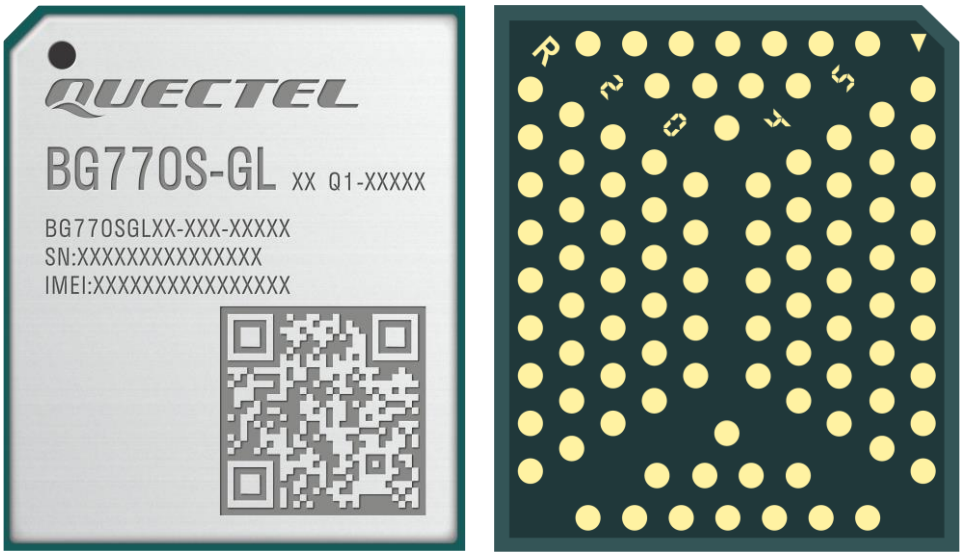


Figure 34: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [20] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[20] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.10–0.13 mm. For more details, see ***document [8]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

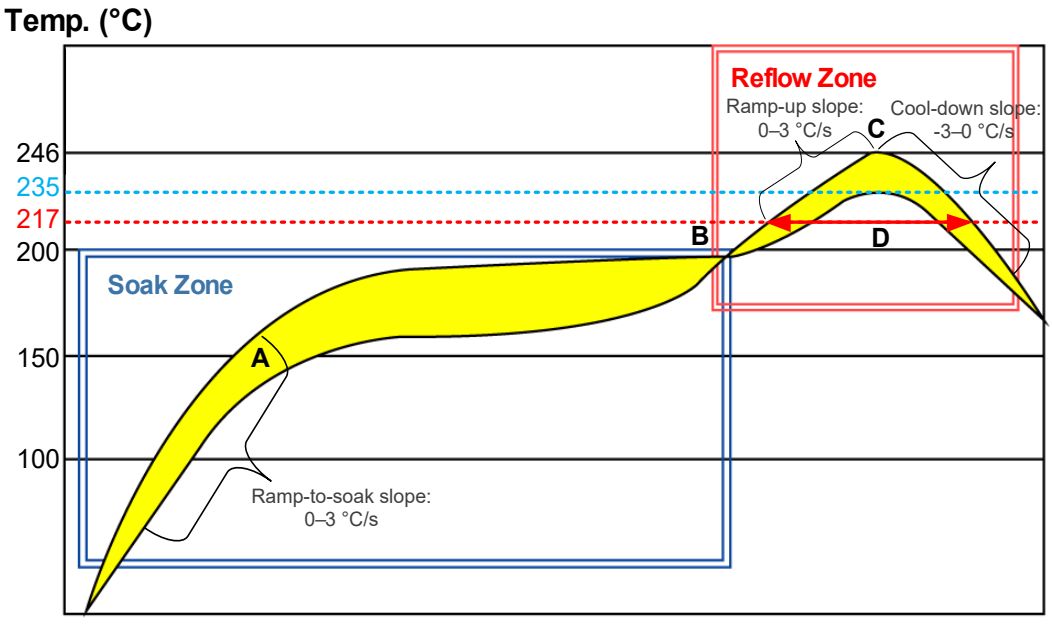


Figure 35: Recommended Reflow Soldering Thermal Profile

Table 44: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
6. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [9]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

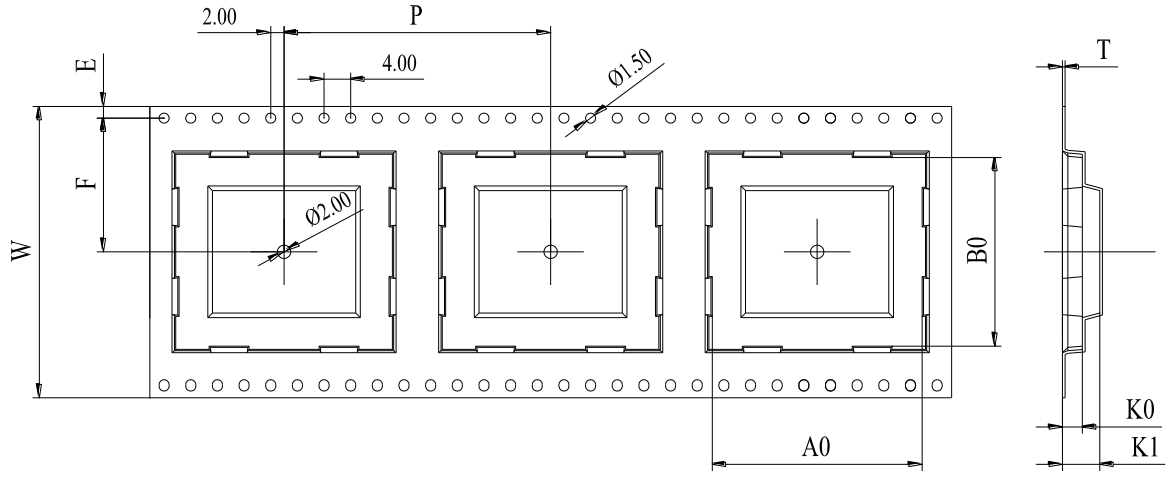


Figure 36: Carrier Tape Dimension Drawing (Unit: mm)

Table 45: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	20	0.35	13.3	15.3	2.35	5.35	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

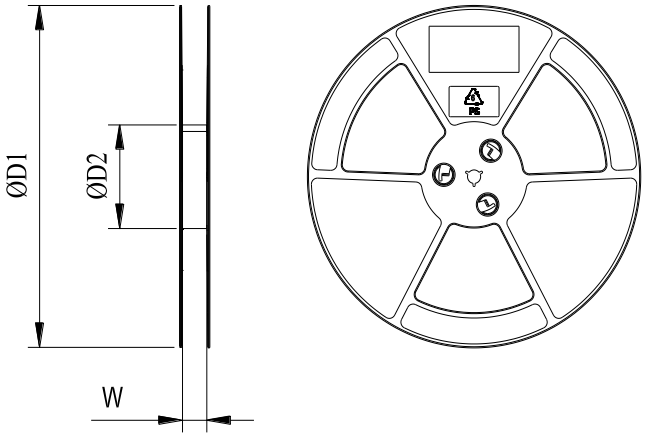


Figure 37: Plastic Reel Dimension Drawing

Table 46: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

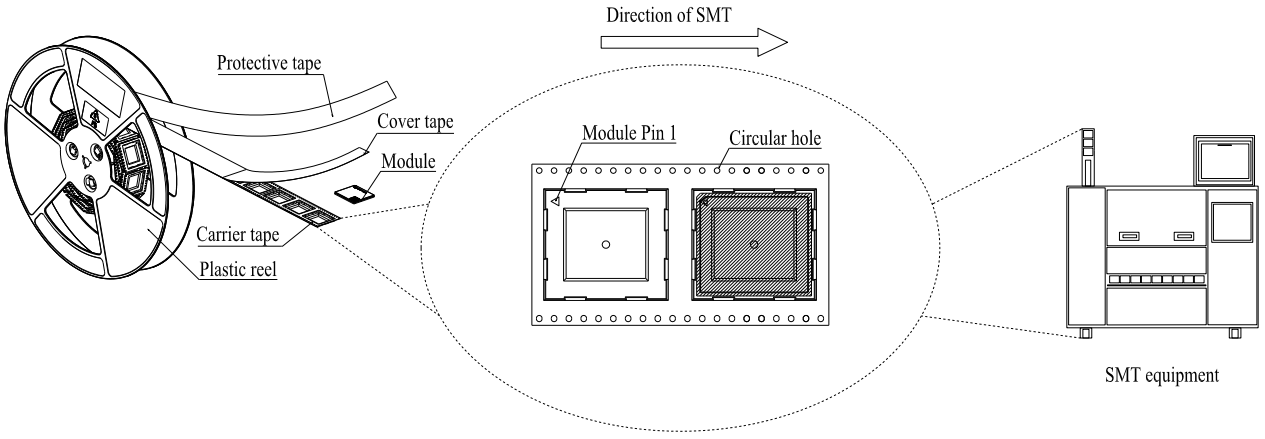
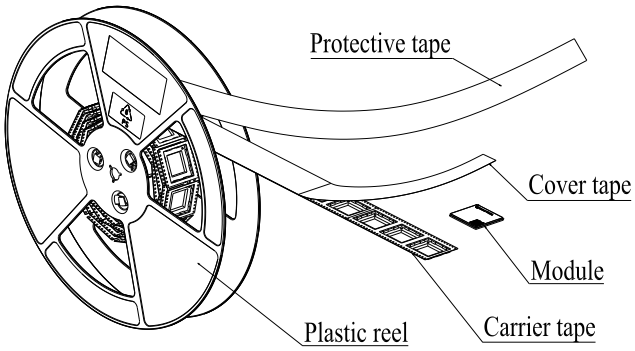


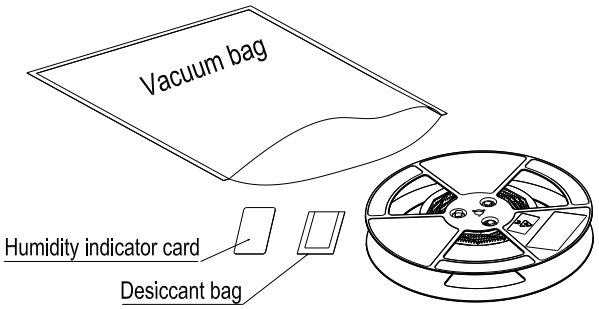
Figure 38: Mounting Direction

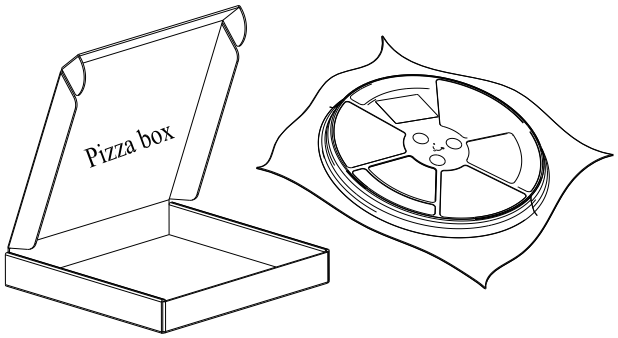
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuum it down.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

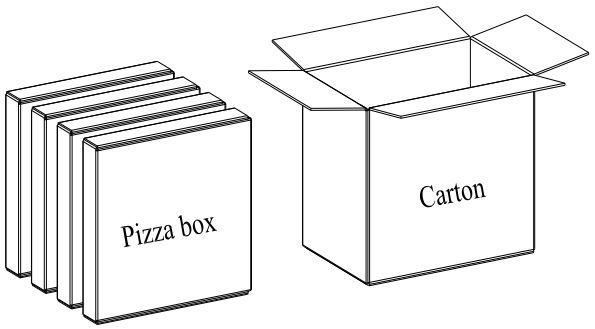


Figure 39: Packaging Process

9 Appendix References

Table 47: Related Documents

Document Name
[1] Quectel_BG770S-GL&BG950S-GL_GNSS_Application_Note
[2] Quectel_BG77xA-GL&BG770S-GL_TE-B_User_Guide
[3] Quectel_BG770S-GL&BG950S-GL_AT_Commands_Manual
[4] Quectel_BG770S-GL&BG950S-GL_Low_Power_Mode_Application_Note
[5] Quectel_BG770S-GL&BG950S-GL_QCFG_AT_Commands_Manual
[6] Quectel_BG770S-GL&BG950S-GL_GNSS_Application_Note
[7] Quectel_RF_Layout_Application_Note
[8] Quectel_Module_Stencil_Design_Requirements
[9] Quectel_Module_SMT_Application_Note

Table 48: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
bps	Bit(s) Per Second
CHAP	Challenge Handshake Authentication Protocol
Cj	Junction Capacitance
CoAP	Constrained Application Protocol
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over the Air

DL	Downlink
DRX	Discontinuous Reception
DTLS	Datagram Transport Layer Security
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FTP(S)	FTP over SSL
FW	Firmware
GNSS	Global Navigation Satellite System
GLONASS	Global Navigation Satellite System (Russia)
GPIO	General-purpose Input/Output
GPS	Global Positioning System
GRFC	Generic RF Controller
HD	Half Duplex
HSS	Home Subscriber Server
HTTP(S)	Hypertext Transfer Protocol Secure
I2C	Inter-Integrated Circuit
IPv4	Internet Protocol version 4
IPv6	Internet Protocol version 6
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low-Power Wide-Area (Network)

LTE	Long Term Evolution
LwM2M	Lightweight M2M
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Chip
MO	Mobile Originated
MOQ	Minimum Order Quantity
MQTT	Message Queuing Telemetry Transport
MRAM	Magnetoresistive Random Access Memory
MSL	Moisture Sensitivity Levels
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDN	Public Data Network
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send

SMD	Surface Mount Device
SMS	Short Message Service
SSL	Secure Sockets Layer
TAU	Tracking Area Update
TBD	To Be Determined
TCP	Transmission Control Protocol
TDM	Time-division Multiplexing
TLS	Transport Layer Security
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network