EG800Z Series QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

Date: 2025-05-26

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an "as available" basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

About the Document

Revision History

Version	Date	Author	Description
-	2025-04-15	George OU/Jaki YU	Creation of the document
1.0	2025-05-26	Mango HUANG/Jaki YU	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG800Z Series module in QuecOpen® solution, including block diagram, power system block diagram, module interfaces, system power supply design, MCU interfaces, UART and USIM interfaces, antenna interface, audio Codec design, audio Codec interface, LCD and camera interfaces, SPI and other designs.
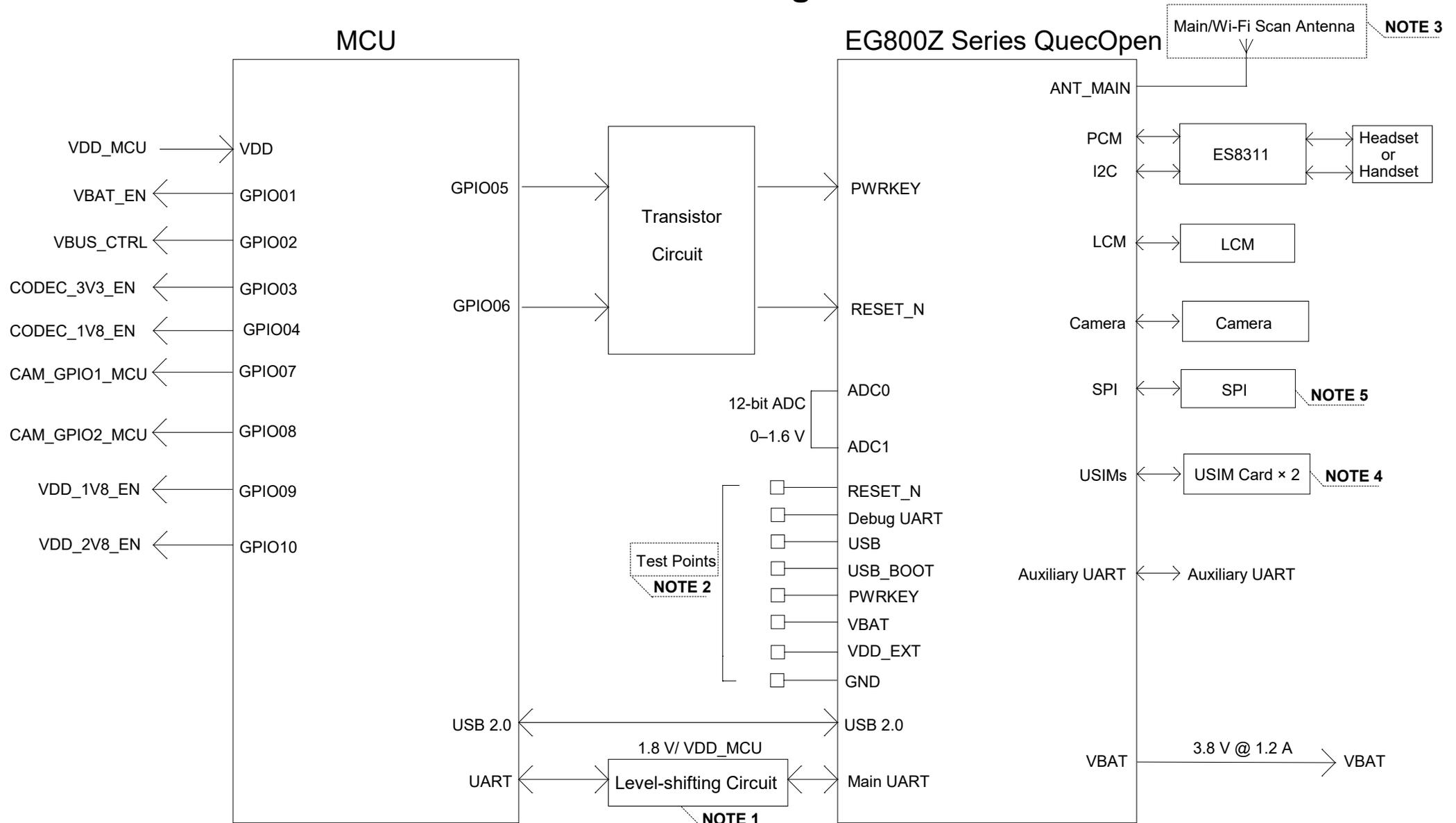
1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram

MCU

EG800Z Series QuecOpen

Main/Wi-Fi Scan Antenna — NOTE 3

VDD_MCU → VDD

ANT_MAIN

VBAT_EN ← GPIO01

PCM ↔ ES8311 ↔ Headset or Handset
I2C

VBUS_CTRL ← GPIO02

CODEC_3V3_EN ← GPIO03

LCM ↔ LCM

CODEC_1V8_EN ← GPIO04

GPIO05 → Transistor Circuit → PWRKEY

CAM_GPIO1_MCU ← GPIO07

Camera ↔ Camera

GPIO06 → RESET_N

CAM_GPIO2_MCU ← GPIO08

SPI ↔ SPI — NOTE 5

12-bit ADC 0–1.6 V — ADC0 / ADC1

VDD_1V8_EN ← GPIO09

USIMs ↔ USIM Card × 2 — NOTE 4

VDD_2V8_EN ← GPIO10

Test Points NOTE 2:
RESET_N
Debug UART
USB
USB_BOOT
PWRKEY
VBAT
VDD_EXT
GND

Auxiliary UART ↔ Auxiliary UART

USB 2.0 ↔ USB 2.0

1.8 V/ VDD_MCU

UART ↔ Level-shifting Circuit NOTE 1 ↔ Main UART
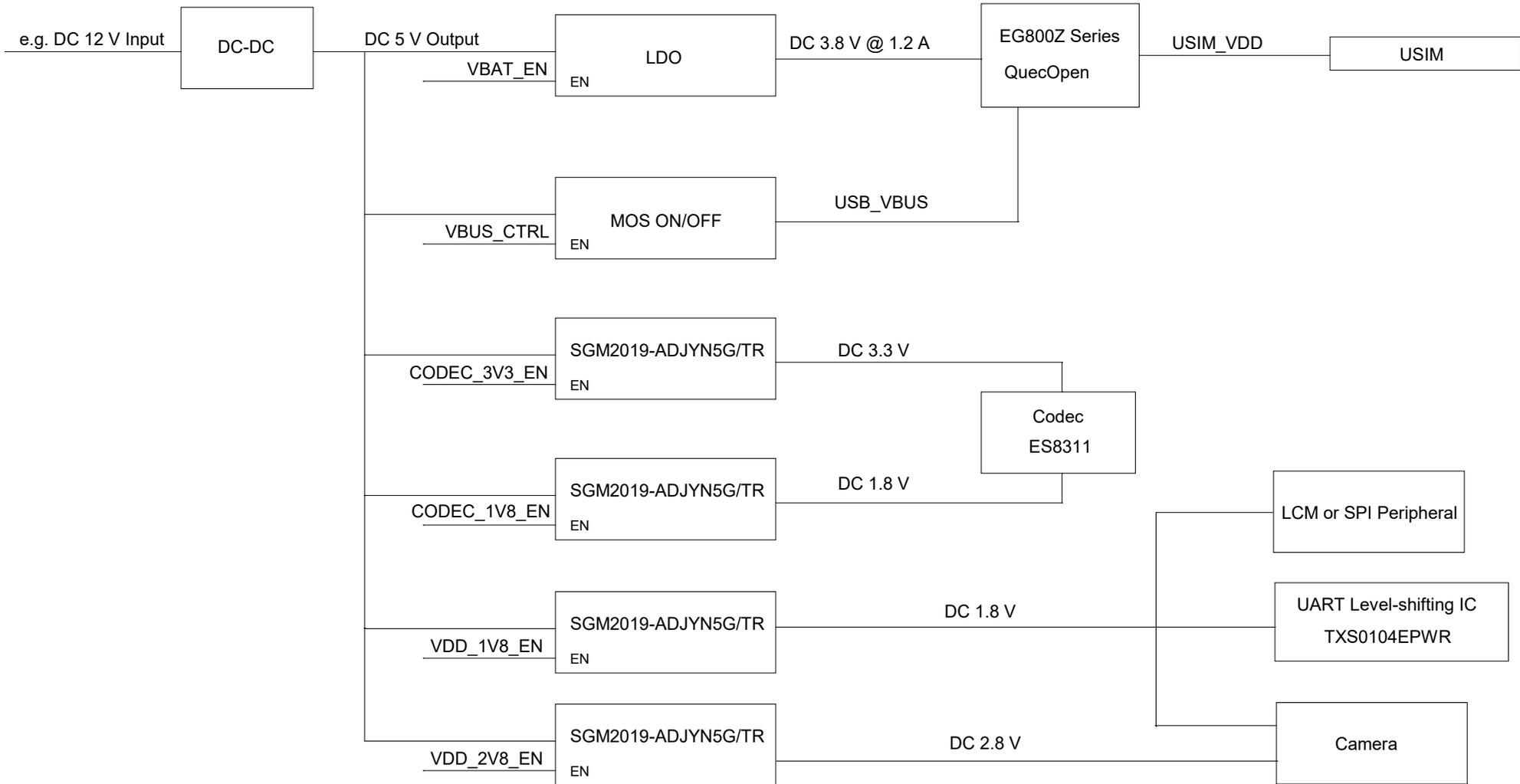
VBAT — 3.8 V @ 1.2 A → VBAT

NOTE:

1. A transistor solution or an IC solution TXS0104EPWR provided by Texas Instruments is recommended.

2. Test points of DBG_TXD/RXD, USB_VBUS, USB_DP/DM, USB_BOOT and VDD_EXT must be reserved. It is recommended to reserve the test points of PWRKEY and VBAT.

   A test point of RESET_N is recommended to be reserved if unused.

3. Wi-Fi scan function and LTE network cannot be used simultaneously since they share the same antenna interface.

4. If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards.

5. The module supports SPI, which can be multiplexed from auxiliary UART and I2C interface. SPI, auxiliary UART and I2C interfaces cannot be used simultaneously.

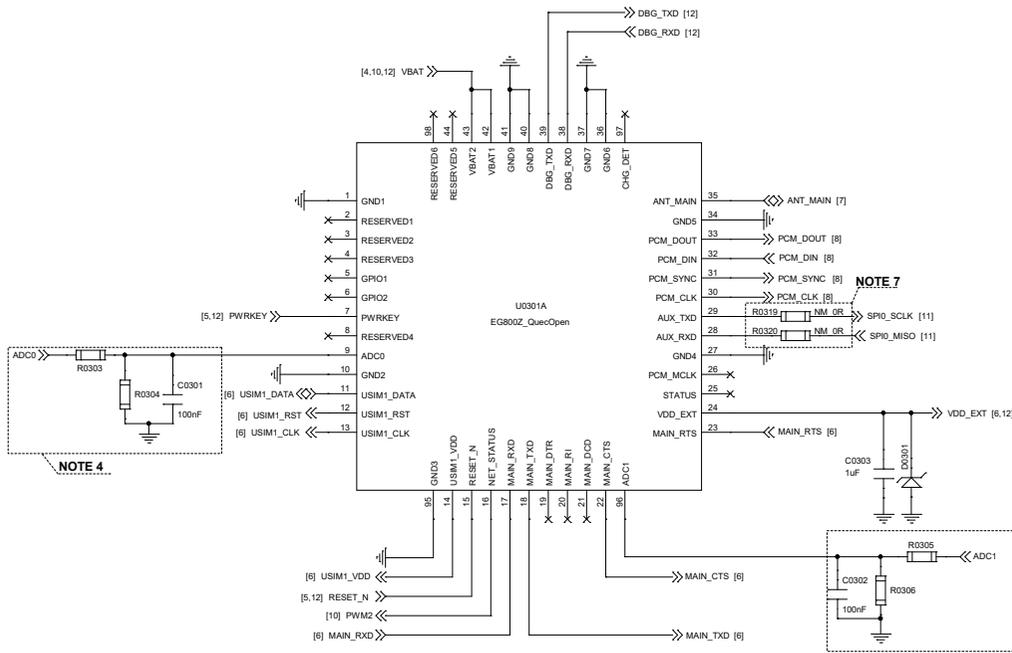   For more details, see the GPIO configuration document of the module.

Power System Block Diagram

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V, 2.8 V and 1.8 V
to power the module, Codec, LCM, SPI, camera and UART level-shifting IC.

e.g. DC 12 V Input → **DC-DC** → DC 5 V Output

LDO (EN, VBAT_EN) → DC 3.8 V @ 1.2 A → **EG800Z Series QuecOpen** → USIM_VDD → **USIM**

MOS ON/OFF (EN, VBUS_CTRL) → USB_VBUS → EG800Z Series QuecOpen

SGM2019-ADJYN5G/TR (EN, CODEC_3V3_EN) → DC 3.3 V → **Codec ES8311**

SGM2019-ADJYN5G/TR (EN, CODEC_1V8_EN) → DC 1.8 V → Codec ES8311

SGM2019-ADJYN5G/TR (EN, VDD_1V8_EN) → DC 1.8 V → **UART Level-shifting IC TXS0104EPWR**

SGM2019-ADJYN5G/TR (EN, VDD_2V8_EN) → DC 2.8 V → **Camera**

LCM or SPI Peripheral

Module Interfaces

U0301A EG800Z_QuecOpen

[4,10,12] VBAT

DBG_TXD [12]
DBG_RXD [12]

GND1 1
RESERVED1 2
RESERVED2 3
RESERVED3 4
GPIO1 5
GPIO2 6
PWRKEY 7 [5,12] PWRKEY
RESERVED4 8
ADC0 9
GND2 10
USIM1_DATA 11 [6] USIM1_DATA
USIM1_RST 12 [6] USIM1_RST
USIM1_CLK 13 [6] USIM1_CLK

ANT_MAIN 35 ANT_MAIN [7]
GND5 34
PCM_DOUT 33 PCM_DOUT [8]
PCM_DIN 32 PCM_DIN [8]
PCM_SYNC 31 PCM_SYNC [8]
PCM_CLK 30 PCM_CLK [8]
AUX_TXD 29 R0319 NM_0R SPI0_SCLK [11]
AUX_RXD 28 R0320 NM_0R SPI0_MISO [11]
GND4 27
PCM_MCLK 26
STATUS 25
VDD_EXT 24 VDD_EXT [6,12]
MAIN_RTS 23 MAIN_RTS [6]

RESERVED6 98
RESERVED5 44
VBAT2 43
VBAT1 42
GND9 41
GND8 40
DBG_TXD 39
DBG_RXD 38
GND7 37
GND6 36
CHG_DET 97

GND3 95
USIM1_VDD 14 [6] USIM1_VDD
RESET_N 15 [5,12] RESET_N
NET_STATUS 16 [10] PWM2
MAIN_RXD 17 [6] MAIN_RXD
MAIN_TXD 18 MAIN_TXD [6]
MAIN_DTR 19
MAIN_RI 20
MAIN_DCD 21
MAIN_CTS 22 MAIN_CTS [6]
ADC1 96

ADC0 R0303 R0304 C0301 100nF

NOTE 4

R0305 ADC1
C0302 R0306 100nF
C0303 1uF D0301

NOTE 4

NOTE 7

U0301B EG800Z_QuecOpen

RESERVED11 106
GND16 72
GND15 71
GND14 70
RESERVED10 69
RESERVED9 68
GRFC2 105

RESERVED7 99
GND10 45
GND11 46
GND12 47
GND13 48
LCD_RST 49 [10] LCD_RST
LCD_SPI_DOUT 50 [10] LCD_SPI_DOUT
LCD_SPI_RS 51 [10] LCD_SPI_RS
LCD_SPI_CS 52 [10] LCD_SPI_CS
LCD_SPI_CLK 53 [10] LCD_SPI_CLK
GPIO3 100

GRFC1 104
I2C_SCL 67
I2C_SDA 66
USIM2_VDD 65 USIM2_VDD [6]
USIM2_DATA 64 USIM2_DATA [6]
USIM2_RST 63 USIM2_RST [6]
USIM2_CLK 62 USIM2_CLK [6]
USB_VBUS 61 USB_VBUS [5,12]
USB_DM 60 USB_DM [5]
USB_DP 59 USB_DP [5]
CAM_RST 103 CAM_RST [10]

NOTE 7
R0318 0R I2C_SCL [8]
R0317 NM_0R SPI0_MOSI [11]
R0316 0R I2C_SDA [8]
R0315 NM_0R SPI0_SSn0 [11]

NOTE 3
R0301 NM_0R USB_DM_TEST [12]
L0301 USB_DM [5]
DLM0NSN900HY2D USB_DP [5]
R0302 NM_0R USB_DP_TEST [12]

GPIO4 101
CAM_MCLK 54 [10] CAM_MCLK
CAM_SPI_DATA0 55 [10] CAM_SPI_DATA0
CAM_SPI_DATA1 56 [10] CAM_SPI_DATA1
CAM_I2C_SCL 57 CAM_I2C_SDA [10]
CAM_I2C_SDA 58 CAM_I2C_SCL [10]
RESERVED8 102

U0301C EG800Z_QuecOpen
GND17 73
RESERVED12 74
RESERVED13 75
RESERVED14 76
RESERVED15 77
LCD_TE 78
USIM1_DET 79 [6] USIM1_DET
CAM_SPI_CLK 80 [10] CAM_SPI_CLK

GND18 88
WAKEUP0 87
RESERVED22 86
RESERVED21 85
RESERVED20 84
RESERVED19 83
USB_BOOT 82 USB_BOOT [12] NOTE 2
CAM_PWDN 81 CAM_PWDN [10]

RESERVED16 107
RESERVED17 108
RESERVED18 109

U0301D EG800Z_QuecOpen
GND19 89
GND20 90
GND21 91
GND24 94
GND23 93
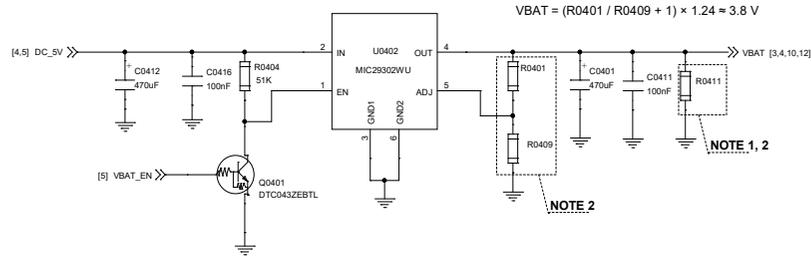GND22 92

NOTE:

1. Connect all GND pins to ground, and keep unused and RESERVED pins unconnected.

2. If the module does not need to enter forced download mode, USB_BOOT cannot be pulled up to VDD_EXT before the module successfully starts up.

3. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI.

   Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.

   Place L0301 and two resistors R0301 and R0302, close to the module to ensure USB signal integrity.

4. The input voltage range of ADC0 and ADC1 interfaces is 0–1.6 V. Please note that the effective input voltage range of ADC interfaces is 0.1–1.5 V.

   There may be relatively large errors in the ranges of 0–0.1 V and 1.5–1.6 V, and it is not recommended to use the ADC interfaces within these ranges.

   When the collected voltage is greater than or equal to 1.5 V, it is recommended to use the resistor divider circuit for ADC application.

   The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.

5. Pins with wake-up interrupt function: WAKEUP0, USB_VBUS, USIM1_DET.

   Pins support wake-up interrupt function only when configured as WAKEUP property pins: GPIO1, GPIO2 and MAIN_DTR.

   MAIN_RXD supports wake-up interrupt function when the module is in PSM or sleep mode.

6. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer.

   Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.

7. The module supports SPI, which can be multiplexed from auxiliary UART and I2C interface. For more details, see the GPIO configuration document of the module.

8. The power domain of the module's GPIO pins is 1.8 V by default and can be configured to 3.3 V. For more details, please contact Quectel Technical Support.
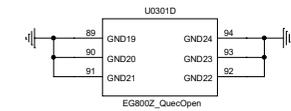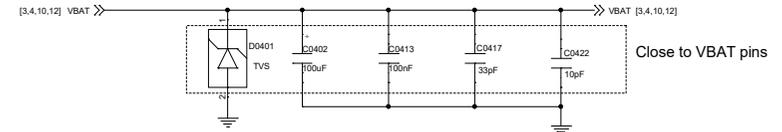
System Power Supply Design

LDO Application

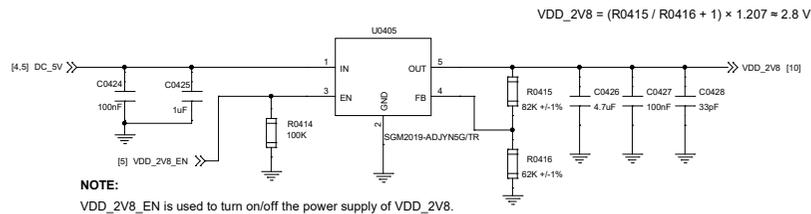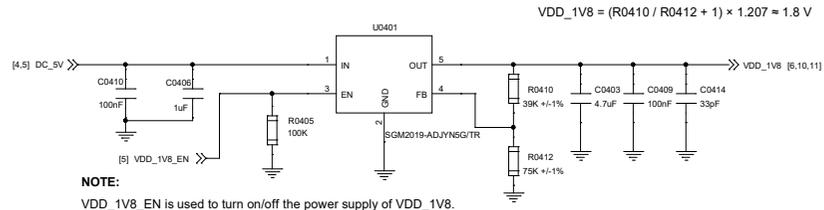When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.

$VBAT = (R0401 / R0409 + 1) \times 1.24 \approx 3.8\ V$

[4,5] DC_5V

C0412 470uF
C0416 100nF
R0404 51K

U0402 MIC29302WU
IN OUT
EN ADJ
GND1 GND2

R0401
R0409

C0401 470uF
C0411 100nF
R0411

VBAT [3,4,10,12]

NOTE 1, 2

[5] VBAT_EN

Q0401 DTC043ZEBTL

NOTE 2

NOTE:

1. The recommended load current should exceed 10 mA.

2. Please adjust the parameters of R0401, R0409 and R0411 in accordance with the actual situation.
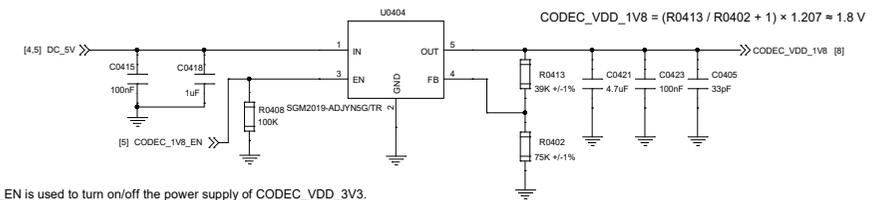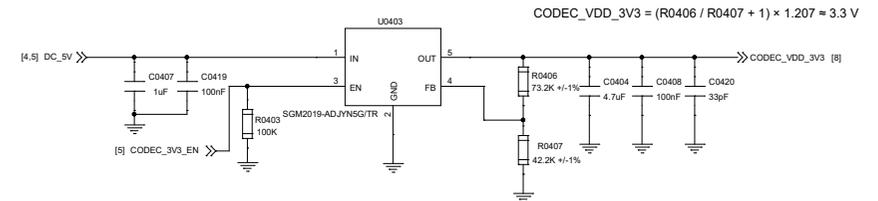
VBAT Design

[3,4,10,12] VBAT

D0401 TVS
C0402 100uF
C0413 100nF
C0417 33pF
C0422 10pF

VBAT [3,4,10,12]

Close to VBAT pins

NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 1.2 A.

2. The width of each VBAT trace should be at least 1.2 mm.

3. The recommended operating voltage range for VBAT is 3.3 V to 4.3 V, with a typical value of 3.8 V.

Power Supply for LCM & Camera & SPI Flash & UART Level-shifting IC

$VDD\_1V8 = (R0410 / R0412 + 1) \times 1.207 \approx 1.8\ V$

[4,5] DC_5V

C0410 100nF
C0406 1uF

U0401
IN OUT
EN FB
GND
SGM2019-ADJYN5G/TR

R0405 100K

R0410 39K +/-1%
C0403 4.7uF
C0409 100nF
C0414 33pF

VDD_1V8 [6,10,11]

R0412 75K +/-1%

[5] VDD_1V8_EN

NOTE:
VDD_1V8_EN is used to turn on/off the power supply of VDD_1V8.

$VDD\_2V8 = (R0415 / R0416 + 1) \times 1.207 \approx 2.8\ V$

[4,5] DC_5V

C0424 100nF
C0425 1uF

U0405
IN OUT
EN FB
GND
SGM2019-ADJYN5G/TR

R0414 100K

R0415 82K +/-1%
C0426 4.7uF
C0427 100nF
C0428 33pF

VDD_2V8 [10]

R0416 62K +/-1%

[5] VDD_2V8_EN

NOTE:
VDD_2V8_EN is used to turn on/off the power supply of VDD_2V8.

Power Supply for PCM Codec

$CODEC\_VDD\_3V3 = (R0406 / R0407 + 1) \times 1.207 \approx 3.3\ V$

[4,5] DC_5V

C0407 1uF
C0419 100nF

U0403
IN OUT
EN FB
GND
SGM2019-ADJYN5G/TR

R0403 100K

R0406 73.2K +/-1%
C0404 4.7uF
C0408 100nF
C0420 33pF

CODEC_VDD_3V3 [8]

R0407 42.2K +/-1%

[5] CODEC_3V3_EN

$CODEC\_VDD\_1V8 = (R0413 / R0402 + 1) \times 1.207 \approx 1.8\ V$

[4,5] DC_5V

C0415 100nF
C0418 1uF

U0404
IN OUT
EN FB
GND
SGM2019-ADJYN5G/TR

R0408 100K

R0413 39K +/-1%
C0421 4.7uF
C0423 100nF
C0405 33pF

CODEC_VDD_1V8 [8]

R0402 75K +/-1%

[5] CODEC_1V8_EN

NOTE:
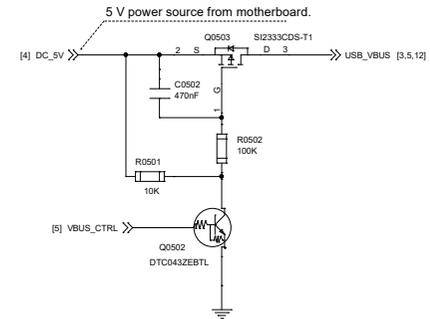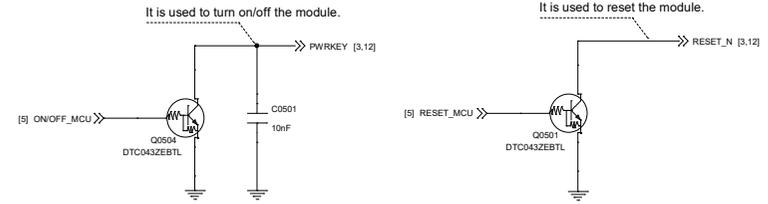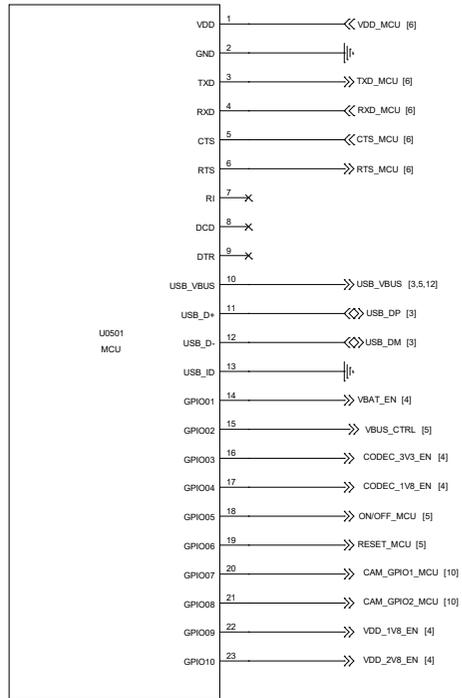
1. CODEC_3V3_EN is used to turn on/off the power supply of CODEC_VDD_3V3.

   CODEC_1V8_EN is used to turn on/off the power supply of CODEC_VDD_1V8.

2. For ES8311 codec, CODEC_VDD_3V3 and CODEC_VDD_1V8 are powered up/down at the same time.

MCU Interfaces

U0501
MCU

Pin	Signal	Net
1	VDD	VDD_MCU [6]
2	GND	
3	TXD	TXD_MCU [6]
4	RXD	RXD_MCU [6]
5	CTS	CTS_MCU [6]
6	RTS	RTS_MCU [6]
7	RI	
8	DCD	
9	DTR	
10	USB_VBUS	USB_VBUS [3,5,12]
11	USB_D+	USB_DP [3]
12	USB_D-	USB_DM [3]
13	USB_ID	
14	GPIO01	VBAT_EN [4]
15	GPIO02	VBUS_CTRL [5]
16	GPIO03	CODEC_3V3_EN [4]
17	GPIO04	CODEC_1V8_EN [4]
18	GPIO05	ON/OFF_MCU [5]
19	GPIO06	RESET_MCU [5]
20	GPIO07	CAM_GPIO1_MCU [10]
21	GPIO08	CAM_GPIO2_MCU [10]
22	GPIO09	VDD_1V8_EN [4]
23	GPIO10	VDD_2V8_EN [4]

It is used to turn on/off the module.

[5] ON/OFF_MCU

Q0504
DTC043ZEBTL

PWRKEY [3,12]

C0501
10nF

It is used to reset the module.

[5] RESET_MCU

Q0501
DTC043ZEBTL

RESET_N [3,12]

5 V power source from motherboard.

[4] DC_5V

Q0503   SI2333CDS-T1
2   S   D   3

USB_VBUS [3,5,12]

C0502
470nF

R0502
100K

R0501
10K

[5] VBUS_CTRL

Q0502
DTC043ZEBTL

NOTE:

1. If the power domain of the module's interfaces is the same as that of the MCU interfaces, the level-shifting circuit is not necessary .

2. The USB interface of the module can only serve as a slave device, and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.

   For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.

3. It is recommended to choose MCU's GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.

UART and USIM Interfaces

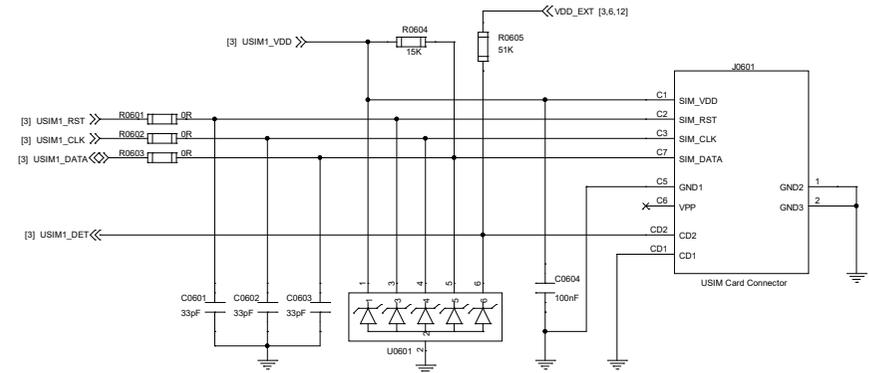## UART Level-shifting Circuit - Transistor Solution

[3,6,12] VDD_EXT

C0605 1nF
R0606 4.7K
R0607 10K

[5,6] TXD_MCU
Q0601 2SC4617TLQ
MAIN_RXD [3,6]

[5,6] VDD_MCU
R0609 4.7K
C0606 1nF
VDD_EXT [3,6,12]
R0608 10K
R0612 10K

[5,6] RXD_MCU
Q0602 2SC4617TLQ
MAIN_TXD [3,6]

UART Level-shifting Circuit - IC Solution

C0607 100nF
U0602
C0608 100nF

[4,6,10,11] VDD_1V8 — 1 VCCA — VCCB 14 — VDD_MCU [5,6]
[3] MAIN_CTS — 2 A1 — B1 13 — CTS_MCU [5]
[3] MAIN_RTS — 3 A2 — B2 12 — RTS_MCU [5]
[3,6] MAIN_RXD — 4 A3 — B3 11 — TXD_MCU [5,6]
[3,6] MAIN_TXD — 5 A4 — B4 10 — RXD_MCU [5,6]
6 NC1 — NC2 9
7 GND — OE 8 — R0610 10K — VDD_1V8 [4,6,10,11]
R0611 120K

TXS0104EPWR

NOTE:

1. There are two level-shifting circuits: transistor solution and IC solution, and it is recommended to select the latter one.

2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0104EPWR.

3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0605 and C0606 of 1 nF can improve the signal quality.

4. If the power domain of MCU is the same as that of the module's UART, and MAIN_TXD is directly connected to the MCU's RXD, the module's MAIN_TXD

   should be pulled up to VDD_EXT via a 10 kΩ resistor to prevent the MCU from receiving error messages when the module is in sleep mode.

5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

6. The above "UART Level-shifting Circuit - IC Solution" are only applicable to the module's 1.8 V UART.

USIM1 Interface Design

R0604 15K
R0605 51K
VDD_EXT [3,6,12]

[3] USIM1_VDD

J0601

[3] USIM1_RST — R0601 0R — C1 SIM_VDD
[3] USIM1_CLK — R0602 0R — C2 SIM_RST
[3] USIM1_DATA — R0603 0R — C3 SIM_CLK
C7 SIM_DATA
C5 GND1 — GND2 1
C6 VPP — GND3 2
[3] USIM1_DET — CD2 CD2
CD1 CD1

C0601 33pF
C0602 33pF
C0603 33pF
C0604 100nF

U0601

USIM Card Connector

USIM2 Interface Design

R0616 15K
R0617 15K

[3] USIM2_VDD

J0602

[3] USIM2_RST — R0615 0R — C1 SIM_VDD
[3] USIM2_CLK — R0614 0R — C2 SIM_RST
[3] USIM2_DATA — R0613 0R — C3 SIM_CLK
C7 SIM_DATA
C5 GND1 — GND2 1
C6 VPP — GND3 2
CD2 CD2
CD1 CD1

C0609 33pF
C0610 33pF
C0611 33pF
C0612 100nF

U0603

USIM Card Connector

NOTE:

1. Only USIM1 interface of the module supports hot-plug detection.

2. It is recommended to use U0601 and U0603 for effective ESD protection with a parasitic capacitance below 15 pF.

3. For USIM1_DATA, USIM2_DATA and USIM2_RST, it is recommended to add 15 kΩ pull-up resistors R0604, R0616 and R0617 near the USIM card connectors

   to improve the anti-jamming capability of the USIM cards.

4. R0601–R0603 and R0613–R0615 are used for debugging, and C0601–C0603 and C0609–C0611 are used for filtering out RF interference.

5. The capacitance of C0604 and C0612 should be less than 1 μF and they should be placed close to the USIM card connectors.

6. If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards.

7. For more information about the layout of USIM interfaces, see the hardware design document of the module.

Antenna Interface

J0701

NOTE 3

R0701
0R

C0703
100pF

ANT_MAIN [3]

D0701
NM

C0701
NM

C0702
NM
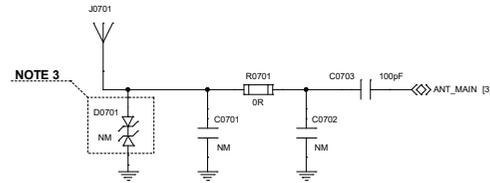
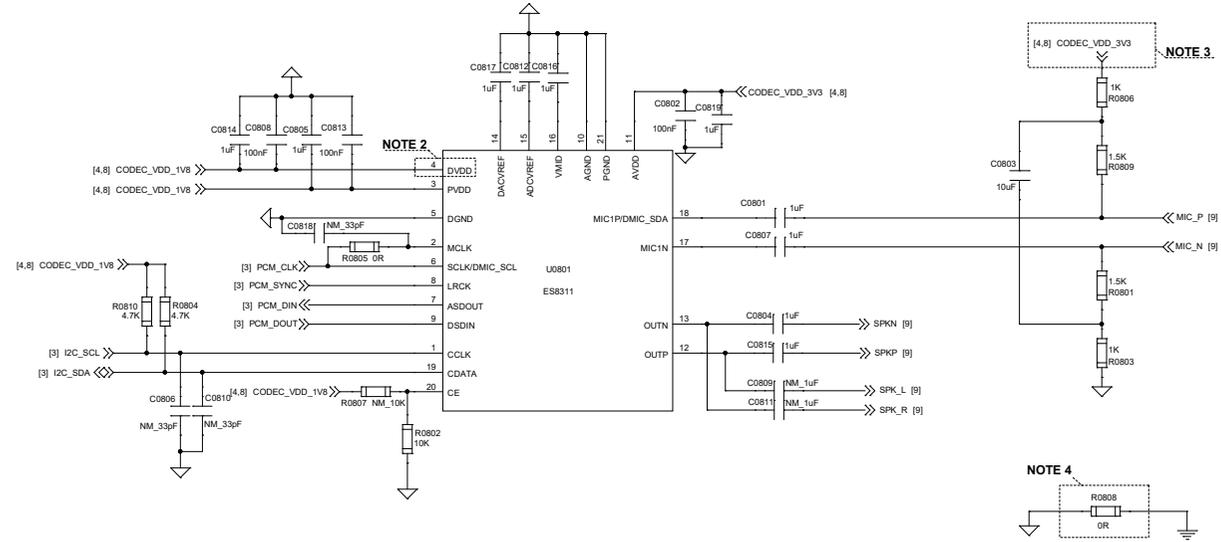**NOTE:**

1. Use a dual L-type matching circuit for the antenna interface.

2. The single-ended impedance of the RF antenna is 50 Ω, and the trace length should be minimized.

3. It is recommended to reserve ESD protection components for the antenna interface and the junction capacitance should not exceed 0.05 pF.

4. Wi-Fi scan function is optional. This function and LTE network cannot be used simultaneously since they share the same antenna interface.

5. Main antenna and Wi-Fi scan only support passive antennas.

6. Notes on C0703:

    1) If there is DC power at the antenna ports, place capacitors on C0703 to prevent short circuit to ground.

      The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.

    2) If there is no DC power in the peripheral design:

      a) Do not reserve C0703.

      b) If C0703 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor.

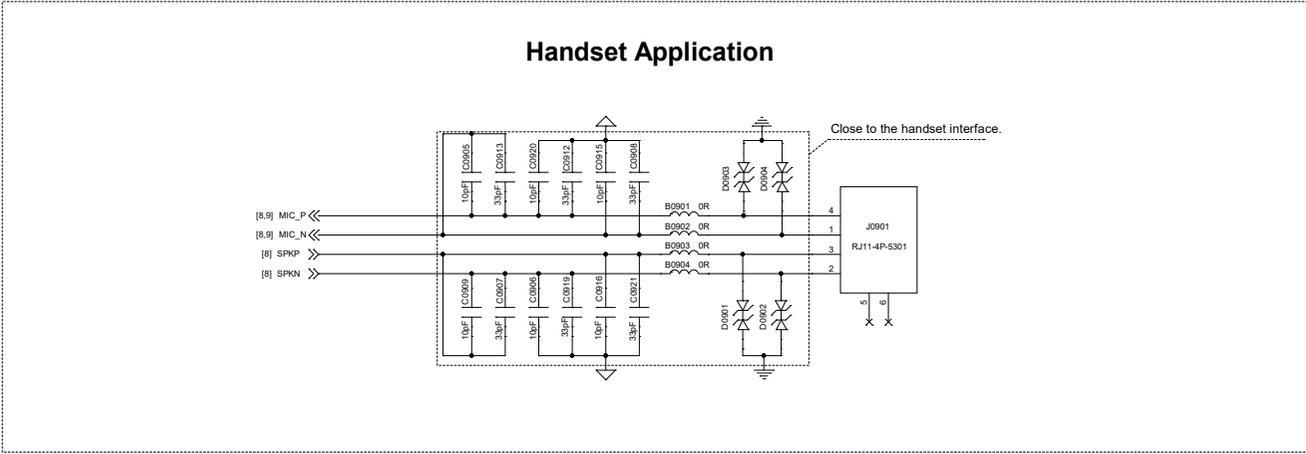   You can also match the component according to the debugging results.

Audio Codec Design (ES8311)

NOTE:

1. ES8311 power-up/down sequences: AVDD, PVDD and DVDD are powered up/down at the same time.

2. When the sampling frequency is 8 kHz and the clock frequency is 512 kHz, DVDD must be connected to 1.8 V.

3. The bias voltage needs to be stable and the ripple should be as small as possible.

4. Differentiate between analog ground and digital ground. Connect analog ground and digital ground using a 0 Ω resistor.

5. The above circuit design is only applicable to the module's 1.8 V PCM and I2C.

6. For more details, see the datasheet of ES8311.

Audio Codec Interface Design

Handset Application

Close to the handset interface.

Headset Application

Close to the headset interface.

	CTIA	OMTP
R0903/R0904	NM	M
R0901/R0902	M	NM
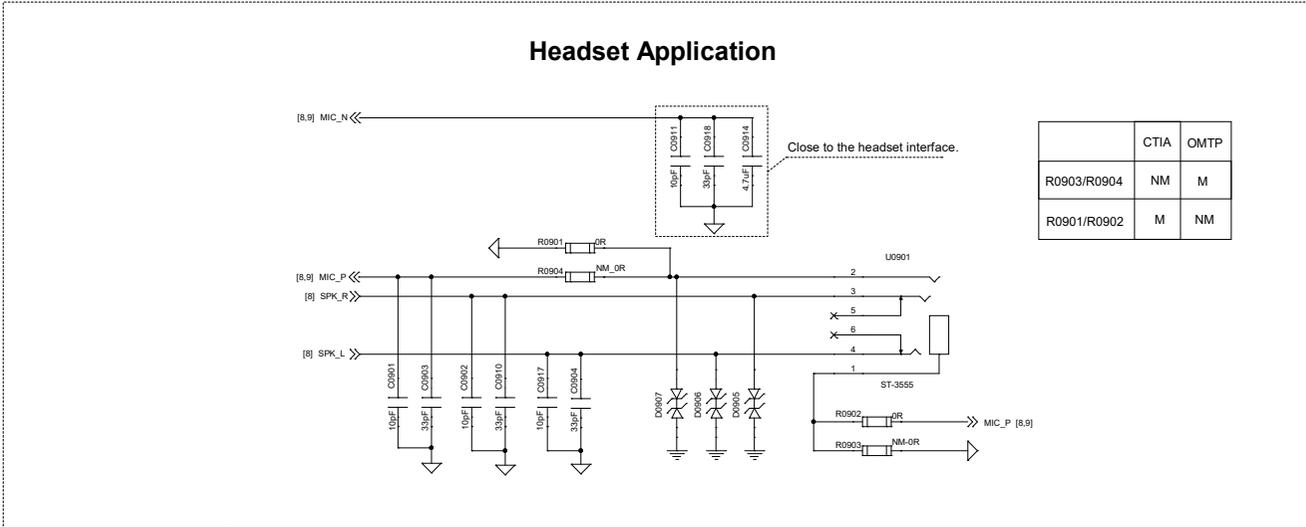
NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, add an audio power amplifier in the design.

2. In handset applications, route the MIC and SPK signal traces as differential pairs.

3. In headset applications, route the MIC signal traces as a differential pair.

4. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference, such as clock and DC-DC signals.

LCM & Camera Interfaces

LCM Interface Design
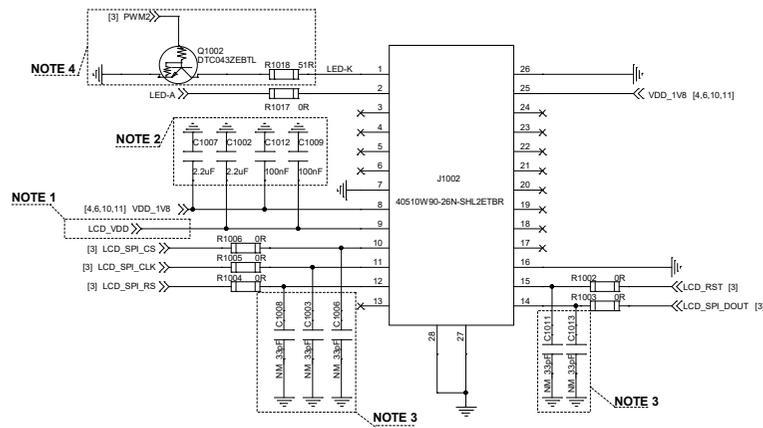
NOTE:

1. It is recommended to design the power supply of LCM interface by yourself.

2. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.

3. Reserve 33 pF capacitors for the signal pins for debugging.

4. The LED-A backlight power supply should be designed by yourself. Select an appropriate resistor (R1018) based on the rated current of the digital transistor and the LED-A voltage value.
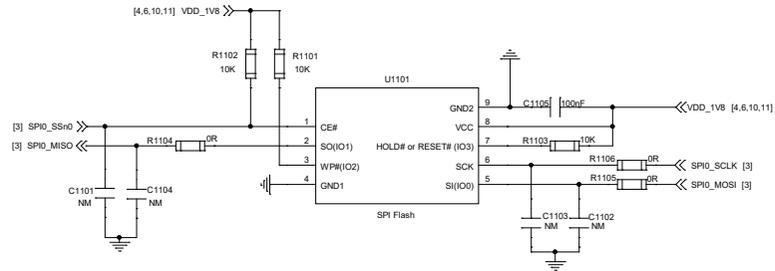
Camera Interface Design
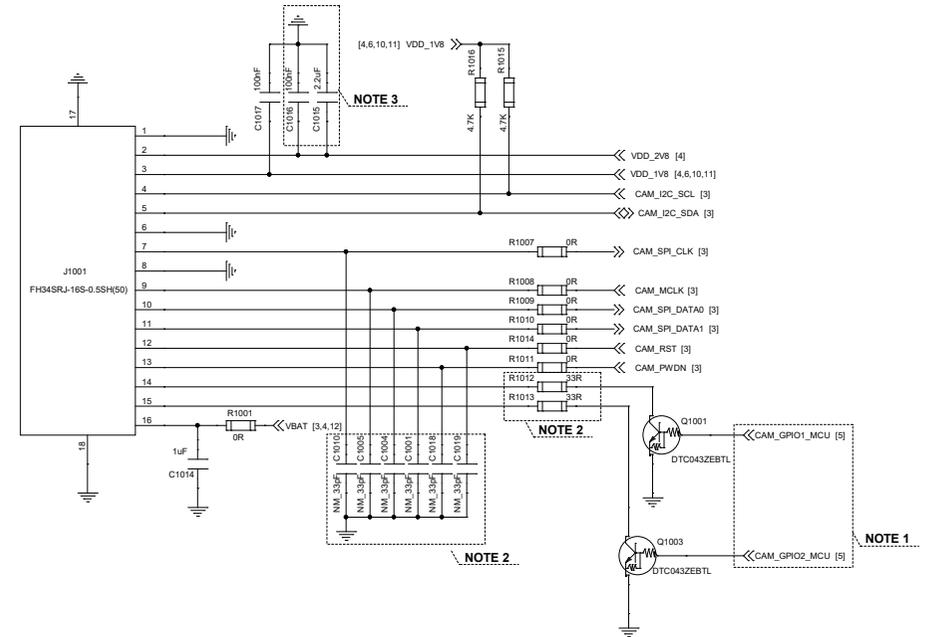
NOTE:

1. To control the cathode of the camera's positioning light, use CAM_GPIO1_MCU with a triode switching circuit. Similarly, CAM_GPIO2_MCU controls the cathode of the camera's supplement light. It is recommended to choose MCU's GPIO pins which are in pull-down status by default as these two control pins.

2. Reserve 33 pF capacitors for the signal pins to facilitate debugging. The values of current limiting resistors (R1012 and R1013) for the positioning light and supplement light should be adjusted based on the required brightness level.

3. Connect the capacitors (C1015 and C1016) of the VDD_2V8 power supply directly to the GND layer. Failing to do so may result in power supply noise causing abnormalities such as white dots on the preview screen.

SPI (Master Mode)

[4,6,10,11] VDD_1V8

R1102 10K   R1101 10K

U1101

[3] SPI0_SSn0	1	CE#	GND2	9
[3] SPI0_MISO	2	SO(IO1)	VCC	8
	3	WP#(IO2)	HOLD# or RESET# (IO3)	7
	4	GND1	SCK	6
			SI(IO0)	5

R1104 0R

C1101 NM   C1104 NM

SPI Flash

C1105 100nF

R1103 10K

VDD_1V8 [4,6,10,11]

R1106 0R   SPI0_SCLK [3]
R1105 0R   SPI0_MOSI [3]

C1103 NM   C1102 NM

NOTE:

1. The module supports SPI, which can be multiplexed from auxiliary UART and I2C interface.

   SPI, auxillary UARTand I2C interfaces cannot be used simultaneously.

   For more details, see the GPIO configuration document of the module.

2. The module's SPI supports master mode only.

Other Designs

Reserved Test Points
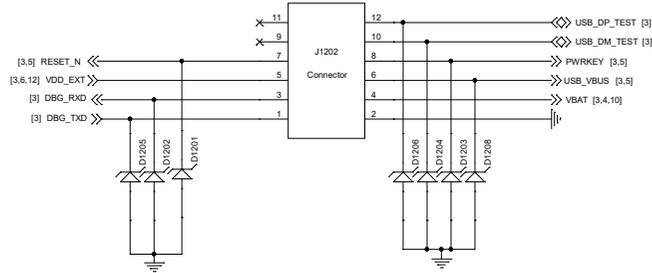
NOTE:

1. Test points of USB interface must be reserved for firmware upgrade, software debugging and log output.

2. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.

3. The debug UART interface supports 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.

Forced Download Interface
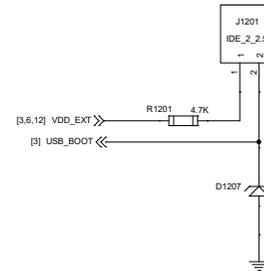
NOTE:

1. Make sure to reserve the forced download interface design and a test point must be reserved for USB_BOOT.

2. Before turning on the module, pull USB_BOOT up to VDD_EXT to activate the forced download mode.

   This mode enables firmware upgrades via the USB interface.