EG800Z Series QuecOpen Hardware Design

LTE Standard Products

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2025-05-21	Mango Huang/ Jaki Yu/ Bronson Zhan	Creation of the document
1.0	2025-06-05	Mango Huang/ Jaki Yu/ Bronson Zhan	First official release
1.1	2026-03-13	Mango Huang/ Jaki Yu/ Charley Jiang	1. Added the applicable module EG800Z-LA and EG800Z-GL. 2. Added a note about applications of frequency bands (Chapter 2.1). 3. Added a note about avoiding abnormal RF functions caused by current sink on the module's pins (Chapter 2.4). 4. Updated the default baud rate supported by debug UART (Table 4 & Table 15). 5. Added information about PWM audio interface (Table 4 & Chapter 4.6). 6. Updated RF transmit power to 23 dBm ±2 dB (Tables 4 & 28). 7. Added a disclaimer of the hazards of not adding TVS (Chapter 3.5.3). 8. Added the trace requirements between the ground of USIM card connector and the module ground (Chapter 4.3). 9. Updated supported baud rates of UART information (Table 15). 10. Added a note about applications of transmit power (Chapter 5.1.2). 11. Updated reference design of RF antenna

	interfaces and added a note about the ESD protection component (Chapter 5.1.4).

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and cost-effectiveness

This document defines the EG800Z series module in QuecOpen® solution and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging.

Table 2: Basic Information

EG800Z Series QuecOpen	
Packaging	LGA
Pin counts	109
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (2.4 ±0.2) mm
Weight	approx. 1.2 g
Wireless network function	LTE/Wi-Fi Scan
Model	● EG800Z-CN ● EG800Z-EU ● EG800Z-LA ● EG800Z-GL

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Mode	EG800Z-CN	EG800Z-EU	EG800Z-LA	EG800Z-GL
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/ B20/B28	B2/B3/B4/B5/B7/B8/ B28/B66	B1/B2/B3/B4/B5/B7 /B8/B12/B13/B14/ B17/B18/B19/B20/ B25/B26/B28/B66/ B71
LTE-TDD	B34/B38/B39/B40/ B41	B38/B40/B41	-	B34/B38/B39/B40/ B41
Wi-Fi Scan	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon

NOTE

1. EG800Z-CN B41 only supports 140 MHz (2535–2675 MHz).
2. The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.
3. The module supports the above frequency bands in hardware, but actual applications may be subject to local regulations.

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: module by default
USB Interface	● Compliant with USB 2.0 specifications (only supports slave mode) ● Data rate: up to 480 Mbps ● Used for data transmission, software debugging, firmware upgrading and outputting logs ● USB Serial Driver: Windows 10/11, Linux 2.6–6.7, Android 4.x–14.x
USIM Interface	● USIM1 supports 1.8 V and 3.0 V USIM cards ● USIM2 only supports 1.8 V USIM cards ● Support Dual SIM Single Standby ● If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards
UART Interfaces	**Main UART:** ● Used for data transmission and firmware upgrades ● Baud rate: 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● When used for log output, the baud rate is 6 Mbps by default **Auxiliary UART:** ● Baud rate: 115200 bps by default

PCM Interface	Used for audio function with external Codec
I2C Interface	● One I2C interface ● Compliant with I2C bus specification
PWM Audio Interface	PWM playback of audio files/streams (recording is not supported)
ADC Interface	● Two ADC interfaces ● Input voltage range: 0–1.6 V
LCM Interface	One LCM interface
Camera Interface	One camera interface supporting cameras up to 0.3 MP
Antenna Interface	● LTE/Wi-Fi Scan antenna interface (ANT_MAIN) ● 50 Ω impedance
Transmit Power	LTE: Class 3 (23 dBm ±2 dB)
LTE Features	● 3GPP Rel-14 FDD and TDD ● Max. LTE category: Cat 1bis ● 1.4/3/5/10/15/20 MHz RF bandwidth ● UL modulations: QPSK, 16QAM ● DL modulations: QPSK, 16QAM and 64QAM ● LTE-FDD: Max. 10 Mbps (DL)/ 5 Mbps (UL) ● LTE-TDD: Max. 8.96 Mbps (DL)/ 3.1 Mbps (UL)
Internet Protocol Features	● TCP/UDP/NITZ/PING/NTP/HTTP/FILE/MQTT/HTTPS/SSL/FTP/FTPS/ CMUX*/MMS/PPP protocols ● PAP and CHAP for PPP connections
Temperature Range	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended operating temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA ● Main UART
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within this range, the module's indicators comply with 3GPP specification requirements.
[2] Within the range of -40 to -35 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts of the module.

- Power management
- Baseband part
- Radio frequency part
- Peripheral interfaces

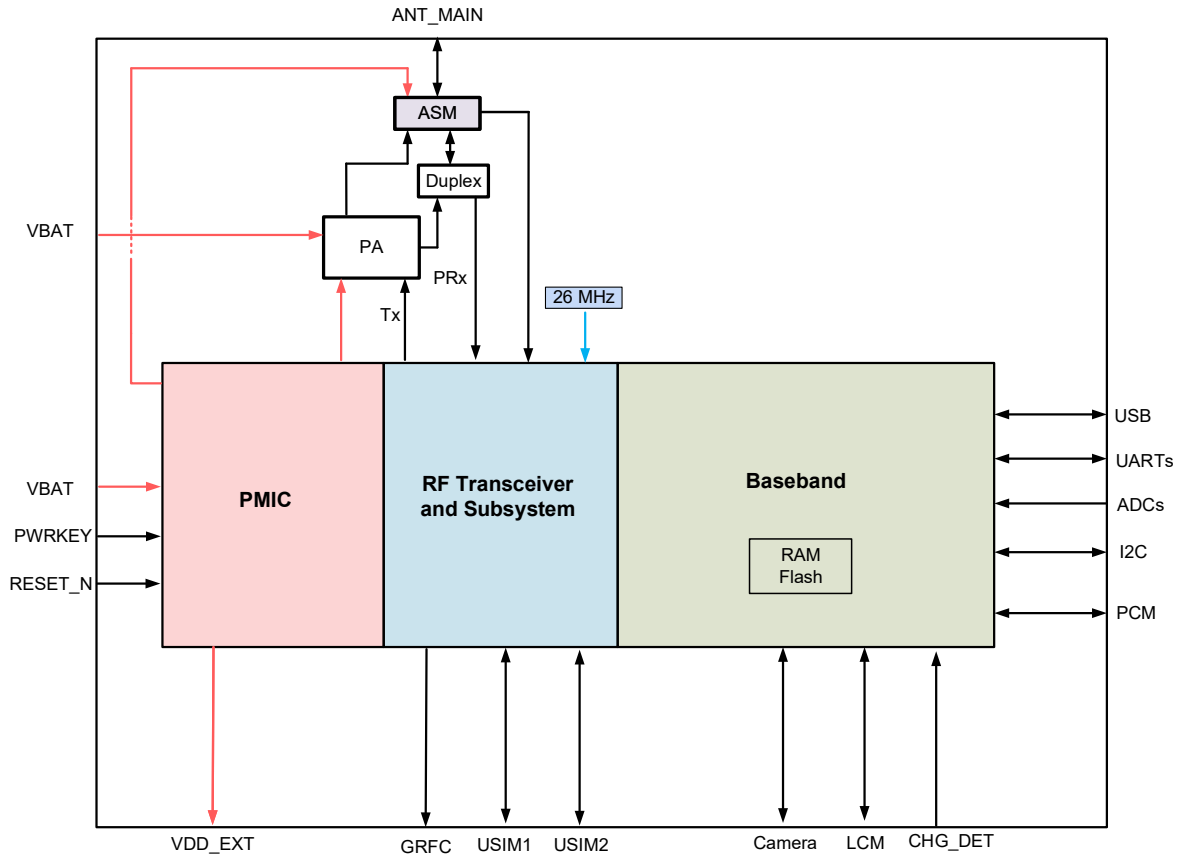


Figure 1: Block Diagram

2.4. Pin Assignment

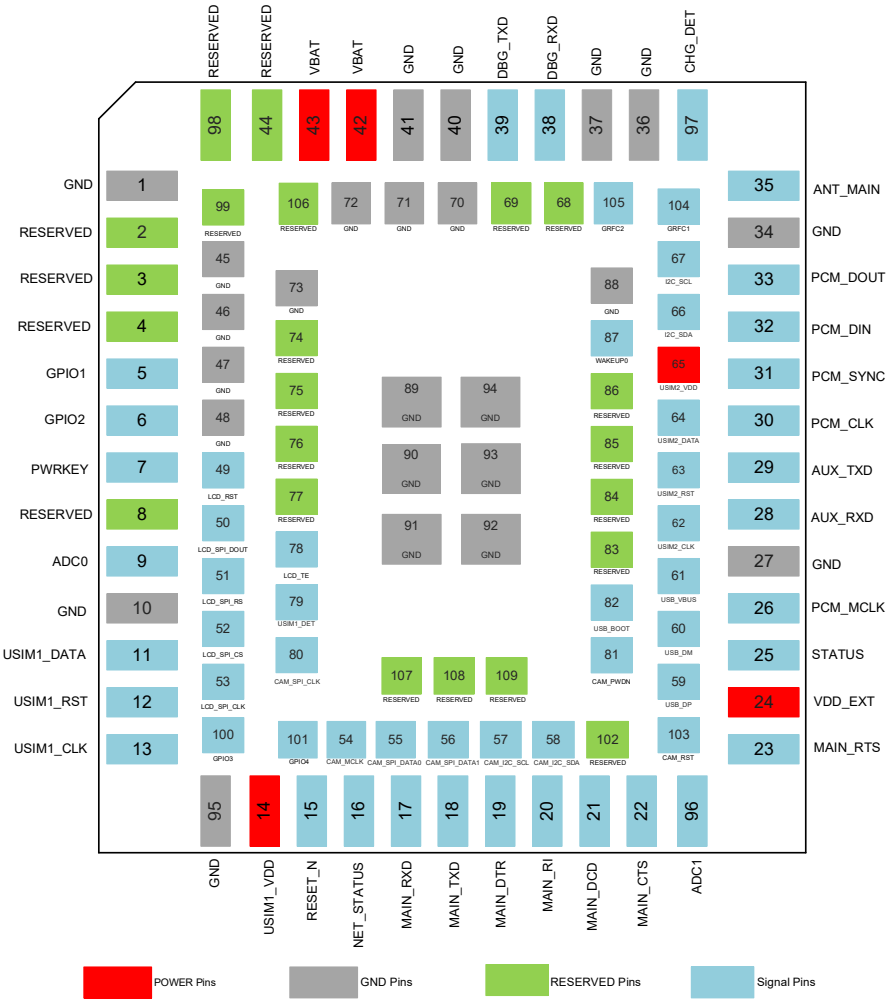


Figure 2: Pin Assignment (Top View)

NOTE

1. If the module does not need to enter forced download mode, USB_BOOT should not be pulled up to VDD_EXT before the module successfully starts up.
2. Please note the following when designing the circuit: In sleep mode, certain module pins will be powered down, including: pins 17 [3], 18, 22 and 23 of main UART, pins 28 and 29 of auxiliary UART, pins 38 and 39 of debug UART, USB_BOOT (pin 82), pins 26, 30–33 of PCM interface, pins 66 and 67 of I2C interface, pins 49–53 and 78 of LCM interface*, pins 54–58, 80, 81 and 103 of camera interface and MAIN_DCD (pin 21). These pins will lose drive capability, halt status indication or data transmission, and any high-level pins may generate periodic pulses during the

[3] If the main UART sleep wake function is enabled by *ql_set_uart_wakeup_enable()*, MAIN_RXD (pin 17) does not power down in sleep mode. For details about the API, refer to ***document [1]***.

paging cycle.
3. Keep all RESERVED pins and unused pins unconnected. Connect all GND pins to the ground.
4. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer. Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.
5. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.
6. For more details about multiplexed functions, see ***document [2]***.

2.5. Pin Definitions

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down
NP	No-pull
H	High level
L	Low level

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	-	Power supply for the module	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	External power supply should be able to provide with sufficient current of 1.2 A. It is recommended to add an external TVS. A test point is recommended to be reserved.
VDD_EXT	24	PO	-	Provide 1.8 V for external pull-ups	Vmax = 1.89 V Vnom = 1.8 V Vmin = 1.71 V $I_O$max = 4 mA	A test point must be reserved. It is necessary to add a 1 μF capacitor and a TVS when designing. It can only be used for external pull-up (pull-up resistance ≥ 4.7 kΩ). The output voltage can be configured to 1.8/3.3V by *ql_gpio_set_voltage()*. For more details, please contact Quectel Technical Support. The pin maintains voltage output even in sleep/PSM mode.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95					Connect these pins to ground.
Turn-on/off						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**

PWRKEY	7	DI	PU	Turn on/off the module	V_{IH}min = 1.7 V V_{IL}max = 1.1 V	After the module is powered up, the voltage is about 1.9 V. Active low. A test point is recommended to be reserved.
RESET_N	15	DI	PU	Reset the module	V_{IH}min = 1.0 V V_{IL}max = 0.3 V	After the module is powered up, the voltage is about 1.15 V. Active low. A test point is recommended to be reserved if unused.
USB Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	61	AI	PD	USB connection detect	Input voltage range: 3.0–5.25 V	A test point must be reserved.
USB_DP	59	AIO	NP	USB 2.0 differential data (+)		Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	60	AIO	NP	USB 2.0 differential data (-)		
USIM Interfaces [4]						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	14	PO	-	USIM1 card power supply	$I_O$max = 34 mA **Low-voltage:** Vmax = 1.89 V Vmin = 1.71 V **High-voltage:** Vmax = 3.15 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.

[4] If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards.

					Vmin = 2.85 V	
USIM1_DATA	11	DIO	PU	USIM1 card data	USIM1_VDD	
USIM1_CLK	13	DO	L	USIM1 card clock		
USIM1_RST	12	DO	H	USIM1 card reset		
USIM1_DET	79	DI	PU	USIM1 card hot-plug detect	V_{IH}min = 1.26 V V_{IL}max = 0.36 V	It is recommended to reserve the RC circuit and pull-up resistor externally. If unused, keep it open.
USIM2_VDD	65	PO	-	USIM2 card power supply	USIM1_VDD **(Low-voltage)**	Share the same power supply with USIM1_VDD.
USIM2_DATA	64	DIO	-	USIM2 card data	VDD_EXT	If USIM2 is used, the level of GPIO pins whose voltage domain is VDD_EXT can only be configured to 1.8 V.
USIM2_CLK	62	DO	-	USIM2 card clock		
USIM2_RST	63	DO	-	USIM2 card reset		
Auxiliary UART Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	29	DO	NP	Auxiliary UART transmit	VDD_EXT	If unused, keep them open.
AUX_RXD	28	DI	NP	Auxiliary UART receive		
Main UART Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	22	DO	NP	Clear to send signal from the module	VDD_EXT	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	NP	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	17	DI	NP	Main UART receive		When the module is in sleep mode and

						PSM, this pin can be used for interrupt wake-up. If unused, keep it open.
MAIN_TXD	18	DO	NP	Main UART transmit		If unused, keep it open.
Debug UART Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	NP	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	39	DO	NP	Debug UART transmit		
I2C Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	67	OD	NP	I2C serial clock	1.8-3.3 V	An external pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	OD	NP	I2C serial data		
PCM Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	31	DO	NP	PCM data frame sync	VDD_EXT	If unused, keep them open.
PCM_CLK	30	DO	NP	PCM clock		
PCM_DIN	32	DI	NP	PCM data input		
PCM_DOUT	33	DO	NP	PCM data output		
PCM_MCLK	26	DO	NP	PCM main clock	VDD_EXT	It is recommended to serve it as the PA enable signal. If unused, keep it open.
Camera Interface						

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
CAM_MCLK	54	DO	NP	Camera master clock	VDD_EXT	If unused, keep them open.
CAM_SPI_DATA1	56	DI	NP	Camera SPI data bit 1		
CAM_SPI_DATA0	55	DI	NP	Camera SPI data bit 0		
CAM_SPI_CLK	80	DO	NP	Camera SPI clock		
CAM_PWDN	81	DO	NP	Camera power down		
CAM_RST	103	DO	PU	Camera reset		
CAM_I2C_SCL	57	OD	PU	Camera I2C clock		An external pull-up resistor is required. If unused, keep them open.
CAM_I2C_SDA	58	OD	PU	Camera I2C data		
LCM Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
LCD_RST	49	DO	NP	LCD reset	VDD_EXT	If unused, keep them open.
LCD_SPI_DOUT	50	DO	NP	LCD SPI data output		
LCD_SPI_RS	51	DO	NP	LCD SPI register select		
LCD_SPI_CS	52	DO	NP	LCD SPI chip select		
LCD_SPI_CLK	53	DO	NP	LCD SPI clock		
LCD_TE	78	DI	NP	LCD tearing effect		
RF Antenna Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN [5]	35	AIO	-	Main antenna/Wi-Fi		50 Ω impedance.

[5] The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.

				Scan antenna interface		
Antenna Tuner Control Interfaces*						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
GRFC1	104	DO	-	General RF control	V_{OH}min = 1.44 V V_{OL}max = 0.27 V	If unused, keep them open.
GRFC2	105	DO	-			
ADC Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	NP	General-purpose ADC interface	Input voltage range: 0–1.6 V	If unused, keep them open.
ADC1	96	AI	NP			
GPIO Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
STATUS	25	DIO	NP	General-purpose input/output	VDD_EXT	Used as GPIO by default.
NET_STATUS	16	DIO	NP			
MAIN_DCD	21	DIO	PU			
MAIN_RI	20	DIO	NP			
MAIN_DTR	19	DI	NP	General-purpose input; external wakeup source	V_{IH}min = 1.26 V V_{IL}max = 0.36 V	If unused, keep them open.
GPIO1	5	DI	NP			
GPIO2	6	DI	NP			
GPIO3	100	DIO	NP	General-purpose input/output	VDD_EXT	It is recommended to use these pins as the PWM* audio output pins. If unused, keep them open.
GPIO4	101	DIO	NP			
Other Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After**	**Description**	**DC Characteristics**	**Comment**

			Reset			
USB_BOOT	82	DI	PD	Force the module into download mode	VDD_EXT	Pull up this pin to VDD_EXT before the module is turned on, the module will enter forced download mode when it is turned on. Active High. A test point must be reserved.
CHG_DET*	97	DI	PU	Charging detection	V_{IH}min = 1.7 V V_{IL}max = 1.1 V	After the module is powered up, the voltage is about 1.9 V. Active Low. If unused, keep it open.
WAKEUP0	87	DI	PU	General-purpose input; external wakeup source	V_{IH}min = 1.26 V V_{IL}max = 0.36 V	If unused, keep it open.
RESERVED						
Pin Name	**Pin No.**					**Comment**
RESERVED	2–4, 8, 44, 68, 69, 74–77, 83–86, 98, 99, 102, 106–109					Keep these pins open.

Some pins of the module are divided into three types: WAKEUP, AGPIO, and AGPIOWU pins. The pin characteristics of these three types are as follows.

Table 7: WAKEUP & AGPIOWU & AGPIO Pin Characteristics

WAKEUP Pins	**Characteristics**
● WAKEUP0 ● USB_VBUS ● USIM1_DET	● Support interrupt wake-up function. ● If the internal pull-up is enabled, the voltage of USIM1_DET and WAKEUP0 is about 1.2 V after the module is turned on. ● It is recommended to reserve an RC circuit and a pull-up resistor externally.
AGPIOWU Pin	**Characteristics**

● GPIO1 ● GPIO2 ● MAIN_DTR	AGPIOWU pins can be configured as WAKEUP or AGPIO pins: ● When configured as WAKEUP pins. – Supports interrupt wake-up function. – If the internal pull-up is enabled, the voltage is about 1.2 V after the module is turned on. – These pins are recommended as the input pins only. – It is recommended to reserve an RC circuit and pull-up resistor externally. ● When configured as AGPIO pins. – Even if the module enters the sleep mode and PSM, the state of these pins will not be affected. – The driving capability of these pins is relatively weak, so they are recommended to be used as input pins only. – The voltage domain is VDD_EXT. For more details, see ***Table 42***.
AGPIO Pins	**Characteristics**
● GPIO3 ● GPIO4 ● STATUS ● NET_STATUS ● MAIN_RI	The state of the pins will not be affected even if the module enters the sleep mode and PSM.

NOTE

1. The power domain of the module's GPIO pins is 1.8 V by default and can be configured to 3.3 V by *ql_gpio_set_voltage()*. For more details, please contact Quectel Technical Support.
2. To reduce the probability of module damage and extend module service life, do not power up and down frequently.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module. For more details, see ***document [3]***.

3 Operating Characteristics

3.1. Operating Modes

Table 8: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	● Executing *ql_dev_set_modem_fun()* sets the module to minimum functionality mode. ● Both RF function and USIM card are invalid.	
Airplane Mode	● Executing *ql_dev_set_modem_fun()* sets the module to airplane mode. ● RF function is invalid.	
Sleep Mode	Power consumption of the module is reduced to an ultra-low level, but the module can still receive paging, SMS and TCP/UDP data from the network.	
PSM	In this mode, the power consumption of the module will be reduced to an extremely low level. The network will be in a non-connected state, and no paging will be received.	
Turn-off Mode	The VBAT pins are constantly turned on and the software stops working.	

NOTE

For more details about *ql_dev_set_modem_fun()*, see ***document [4]***.

3.2. PSM

The module supports PSM (power saving mode). When the module works normally, you can enable PSM via *ql_psm_sleep_enable()* and *ql_autosleep_enable()*. The module can be awakened from PSM by any of the following methods:

- Wake-up by TAU periodic request timer (T3412).
- Wake-up by driving PWRKEY pin low.
- Wake-up by sending data through main UART.
- Wake-up by WAKEUP property pins.

NOTE

For details about PSM related API, refer to ***document [5]*** and ***document [6]***.

3.3. Sleep Mode

The power consumption of the module is reduced to an ultra-low level during sleep mode.

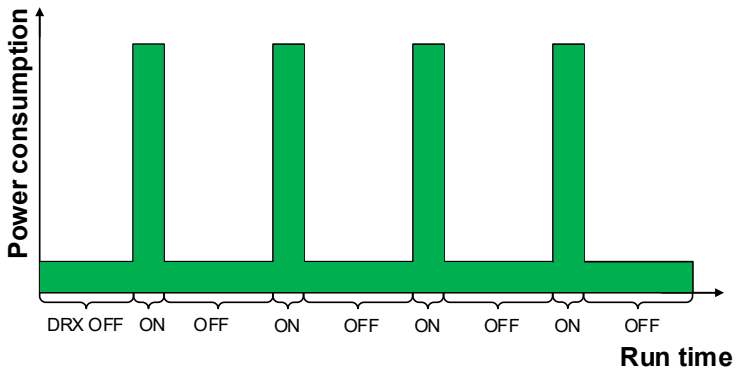


Figure 3: Power Consumption During Sleep Mode

NOTE

The DRX period value is sent by the base station over the wireless network.

3.3.1. UART Application Scenario

If the MCU communicates with the module main UART interface, execute *ql_autosleep_enable()* to make the module enter sleep mode.

The figure illustrates the connection between the module and the MCU.

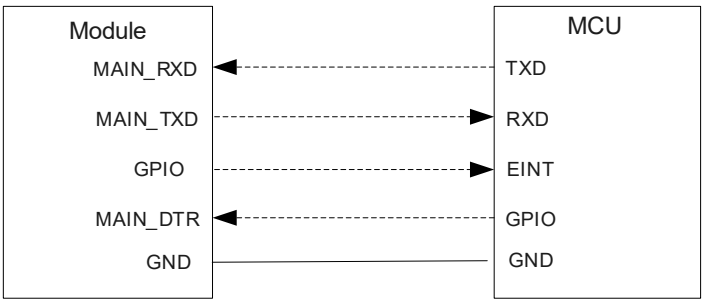


Figure 4: Sleep Mode Application via UART

- The module can be woken up by the MCU through WAKEUP property pins.
- If the wakeup interrupt function of MAIN_RXD is enabled by *ql_set_uart_wakeup_enable()*, the module can be woken up by sending data to the MAIN_RXD (if the baud rate of main UART is higher than 9600 bps, this data will be lost). For more information about API, refer to ***document [5]***.

3.3.2. USB Application Scenarios

3.3.2.1. With USB Suspend/Resume and USB Remote Wakeup Function*

The host supports USB Suspend, Resume and remote wakeup function. Three preconditions should be met to make the module enter sleep mode.

- Execute *ql_autosleep_enable()*.
- Ensure that all sleep locks have been released.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The figure illustrates the connection between the module and the host.

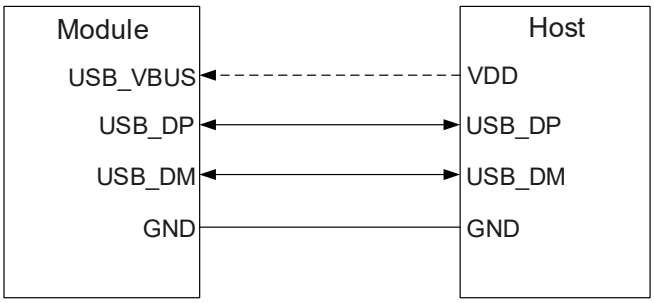


Figure 5: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

Sending data to the module through USB will wake up the module.

3.3.2.2. Without USB Suspend Function

If the host does not support USB Suspend function, the module can enter sleep mode by disconnecting USB_VBUS via an external control circuit.

- Execute *ql_autosleep_enable()*.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Make sure all sleep locks have been released
- Disconnect the USB_VBUS power supply.

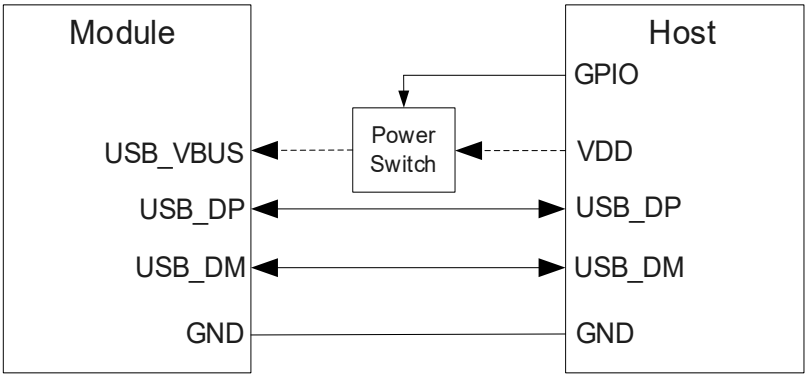


Figure 6: Block Diagram of Application without USB Suspend Function in Sleep Mode

Restoring the supply power of USB_VBUS will wake up the module.

NOTE

1. Note the level matching between signals connected between modules and MCU/ host in ***Chapter 3.3***.
2. For more information about API, refer to ***document [5]***.

3.4. Airplane Mode

When the module enters airplane mode, the RF function is disabled and all related APIs cannot be executed.

This mode can be set through *ql_dev_set_modem_fun()*, which allows you to choose the functionality level through setting *at_dst_cfun* as 0, 1 or 4.

- *at_dst_cfun* is 0: Minimum functionality mode. (Both RF and USIM functions are disabled)
- *at_dst_cfun* is 1: Full functionality mode. (Default).
- *at_dst_cfun* is 4: Airplane mode. (RF function is disabled)

NOTE

For more information about the API, refer to ***document [4]***.

3.5. Power Supply

3.5.1. Power Supply Interfaces

The module has two VBAT pins for connecting to external power supply.

Table 9: Pin Description of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	PI	Power supply for the module	3.3	3.8	4.3	V
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95						

3.5.2. Reference Design for Power Supply

Power supply design is essential for module performance. It is recommended to be provided with sufficient current of 1.2 A to the module. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

A reference design for +5 V input power source is illustrated in the following figure (Please adjust the parameters in accordance with the actual situation).

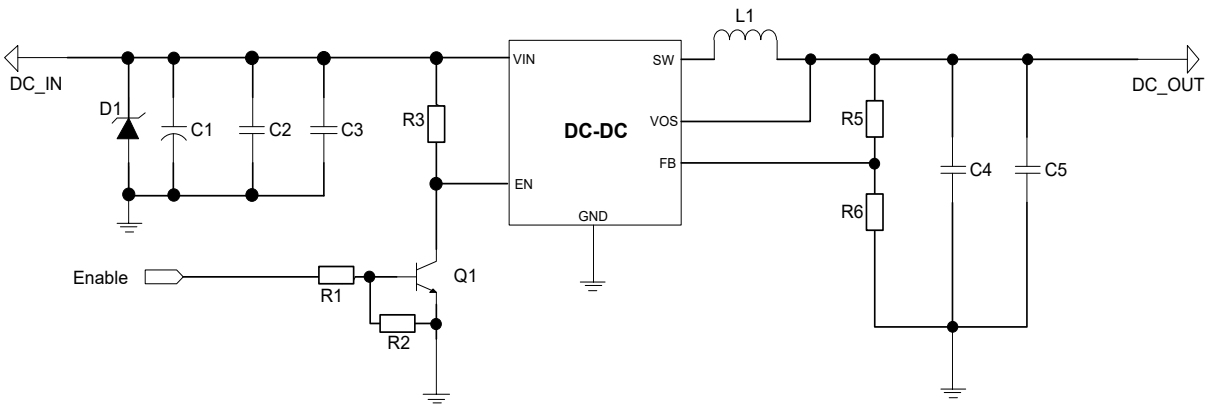


Figure 7: Power Supply Reference Design

3.5.3. Requirements for Voltage Stability

The power supply range of the module is 3.3–4.3 V. Make sure the input voltage never drops below 3.3 V. During the process in network search or data transmission, the input voltage should not fall below the module's minimum operating voltage of 3.3 V. Failure to maintain this voltage may result in module malfunction or unstable operation.

To decrease the voltage drop, use a bypass capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω). A multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR is recommended. Use three ceramic capacitors (100 nF, 33 pF and 10 pF) to compose the array and place them close to VBAT pins. The width of VBAT trace should be at least 1.2 mm. In principle, the longer the VBAT trace is, the wider it should be.

To ensure the stability of the power supply, add a TVS with V_{RWM} = 4.7 V, low clamping voltage and high reverse peak pulse current I_{PP} at the front end of the power supply. If TVS is not added, surges on the input power supplies may cause damage to the module. The reference design is shown as below.

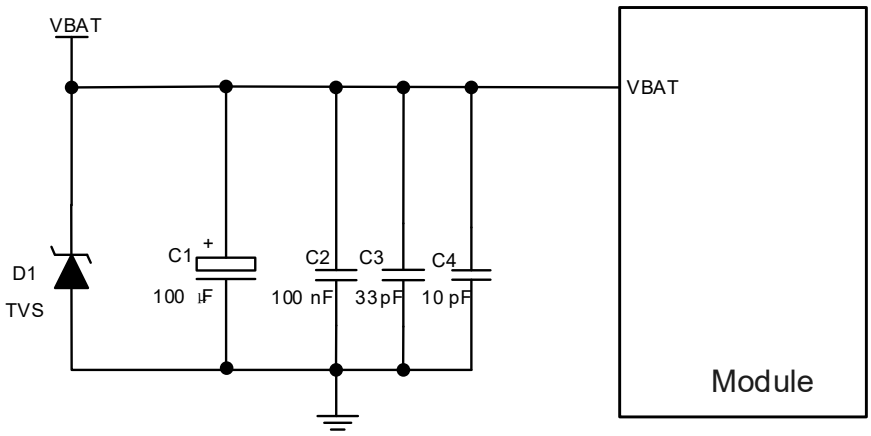


Figure 8: Power Supply Reference Design

3.6. Turn-on

3.6.1. Turn-on with PWRKEY

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	After the module is powered up, the voltage is about 1.9 V.

	Active low. A test point is recommended to be reserved.

When the module is in turn-off mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open collector driver to control the PWRKEY.

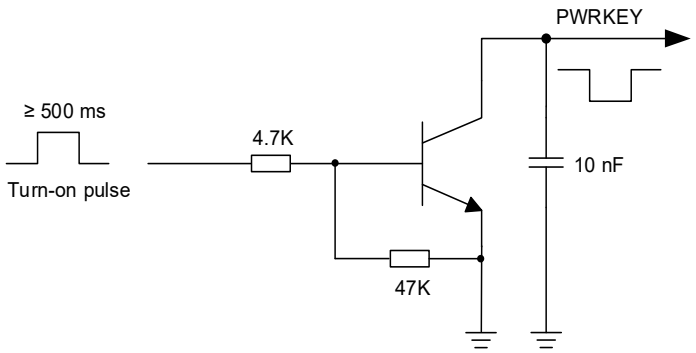


Figure 9: Reference Design of Turning on the Module with Driving Circuit

NOTE

Ensure that the capacitances connected to PWRKEY do not exceed 10 nF.

The module can also be turned on by pressing the PWRKEY button. A TVS diode should be placed near the button for protection against ESD.

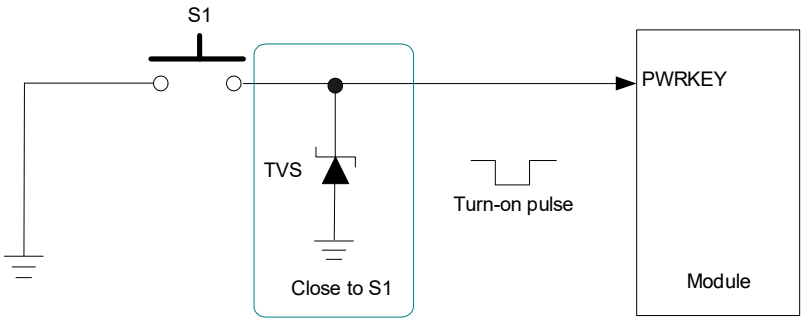


Figure 10: Reference Design of Turning on Module with Keystroke

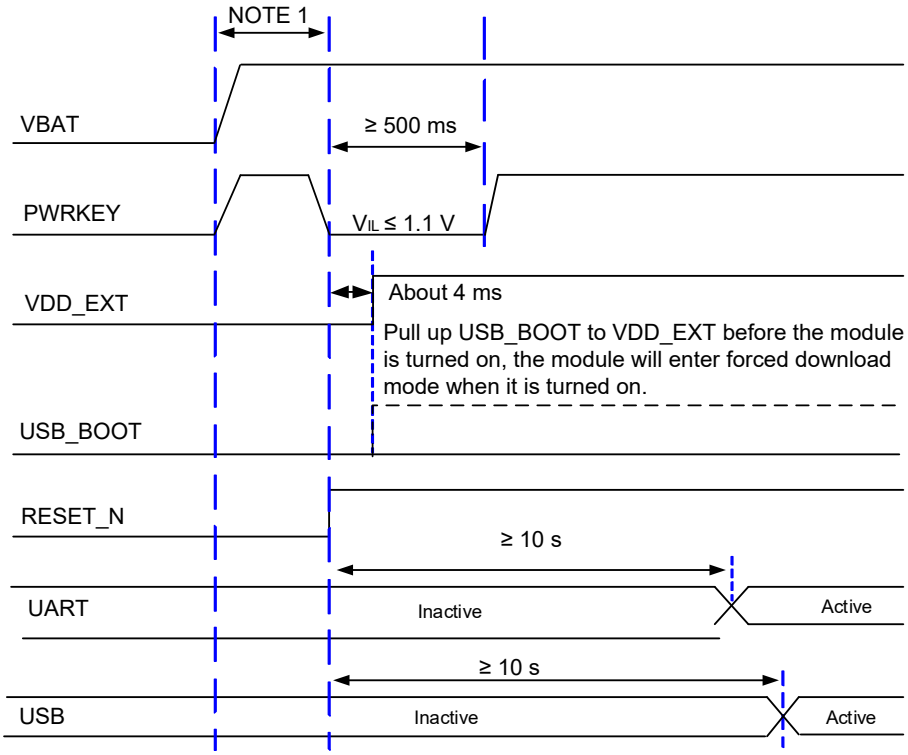


Figure 11: Turn-on Timing

NOTE

1. The PWRKEY pin is internally pulled up through a resistor with approximately 130 kΩ resistance inside the module.
2. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
3. If the module needs to turn on automatically, you can drive PWRKEY pin low by connecting it directly to the ground with resistor not exceeding 4.7 kΩ (4.7 kΩ is recommended by default), or by using a GPIO of an external MCU to drive PWRKEY low before the module powers up (PWRKEY needs to remain at low level after the module is turned on). Besides, before the module is turned on, it is necessary to ensure that the voltage of VBAT pin of the module is lower than 0.5 V.

3.7. Turn-off

3.7.1. Turn-off with PWRKEY

The module will execute turn-off procedure if you drive the PWRKEY pin low for at least 650 ms and then release it.

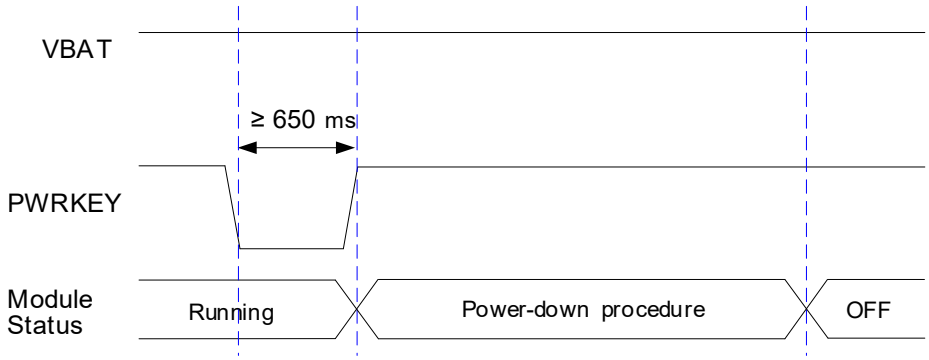


Figure 12: Turn-off Timing with PWRKEY

3.7.2. Turn-off with API

You can execute *ql_power_down()*, to turn off the module, which is the same as turning off the module via the PWRKEY pin. See ***document [7]*** for details about API.

NOTE

1. When turning off the module with the API, keep PWRKEY at high level after the execution of the command. Otherwise, the module cannot be turned off.
2. When PWRKEY is pulled down to the ground, API cannot be used to turn off the module.

3.8. RESET_N

Drive RESET_N low for at least 300 ms and then release it to reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	After the module is powered up, the voltage is about 1.15 V. Active low. A test point is recommended to be reserved if unused.

You can use an open collector driver to control RESET_N. The off-state leakage current of the selected triode should be less than 0.5 μA.

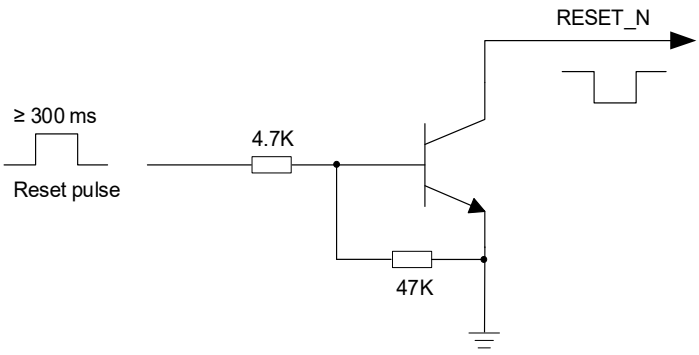


Figure 13: Reference Design of RESET_N with Driving Circuit

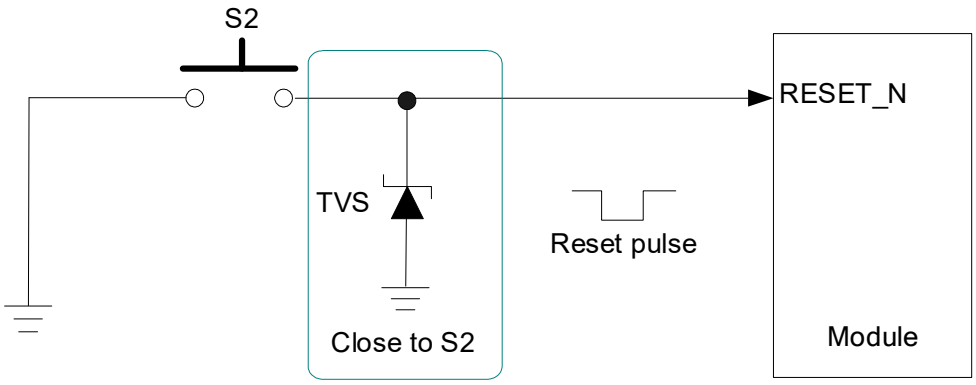


Figure 14: Reference Design of key reset with Driving Circuit

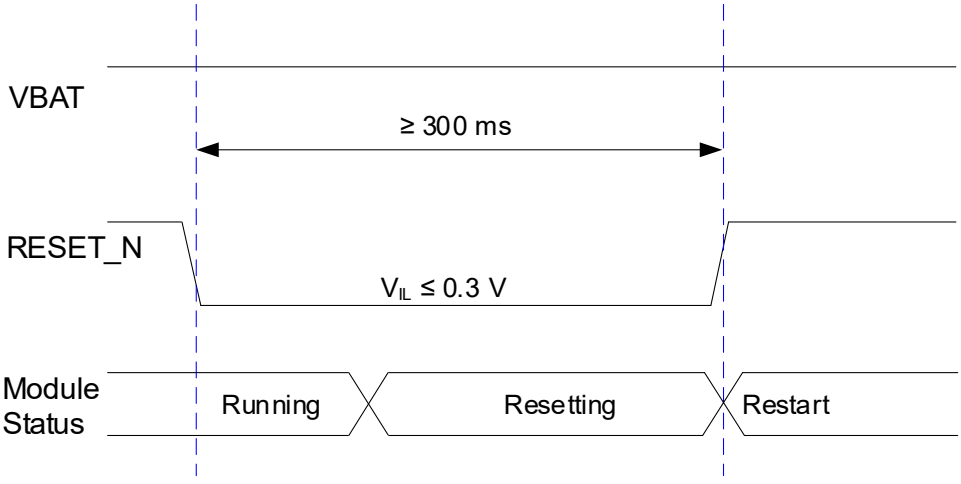


Figure 15: Reset Timing

NOTE

1. The RESET_N pin is internally pulled up through a resistor with approximately 80 kΩ resistance inside the module.
2. It is recommended to use the RESET_N reset function only after both the API and PWRKEY shutdown fail.
3. Ensure that the capacitances connected to RESET_N do not exceed 10 nF.

4 Application Interfaces

4.1. USB Interface

The module has one USB interface, which complies with the USB 2.0 specifications, and supports high speed (480 Mbps) and full speed (12 Mbps) on USB 2.0. The module only supports USB slave mode. The USB interface can be used for data transmission, software debugging, firmware upgrades and logs output.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	61	AI	USB connection detect	A test point must be reserved.
USB_DP	59	AIO	USB 2.0 differential data (+)	Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)	

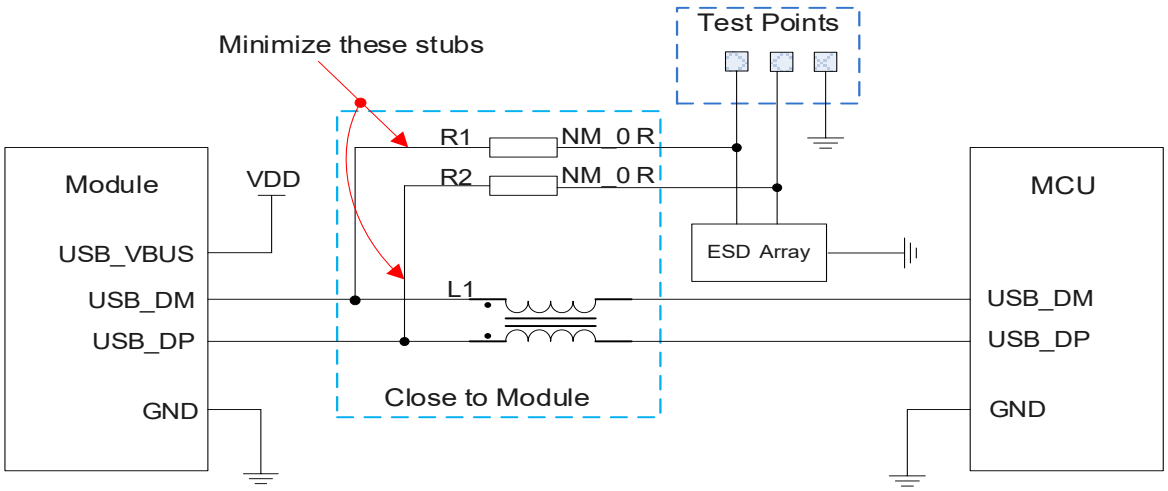


Figure 16: Reference Circuit of USB Interface

It is recommended to add a common-mode choke L1 in series between the module and MCU to suppress EMI. In addition, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points for debugging. These resistors are not mounted by default. To ensure USB data transmission integrity, L1, R1 and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. Extra trace stubs must be as short as possible.

To ensure performance, you should follow the following principles when designing a USB interface:

- Route the USB signal traces as differential pairs surrounded by ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in an inner layer of the PCB, and surround the traces with ground on the same layer and with ground planes above and below.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, the stray capacitance should be less than 2 pF.

For more details about the USB specifications, visit http://www.usb.org/home.

NOTE

Test points must be reserved for USB ports to obtain logs and locate customer problems.

4.2. Forced Download Interface

The module has a USB_BOOT for forced download. Pull up USB_BOOT to VDD_EXT before the module is turned on, the module will enter forced download mode when it is turned on. In this mode, the module can be upgraded via USB 2.0 interface.

Table 13: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	82	DI	Force the module into download mode	Active High. A test point must be reserved.

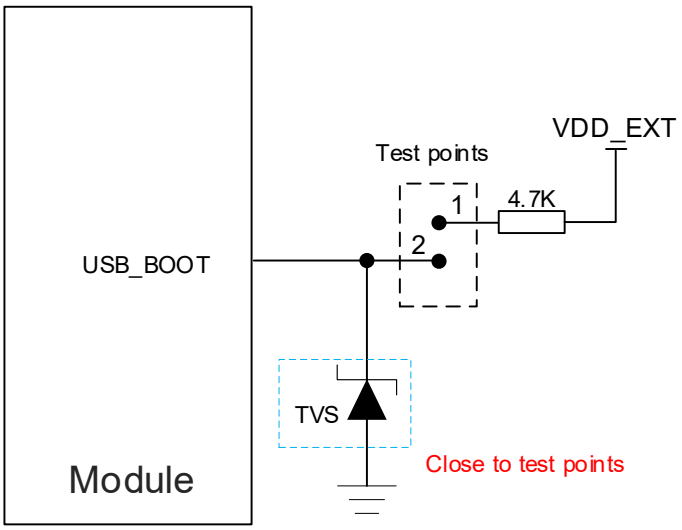


Figure 17: Reference Design of USB_BOOT Interface

4.3. USIM Interfaces

The module has two USIM interfaces, which meet ETSI and IMT-2000 requirements and support Dual Sim Single Standby. USIM1 interface supports 1.8 V and 3.0 V USIM cards; USIM2 interface only supports 1.8V USIM cards.

In Dual SIM Single Standby or single USIM2 usage scenarios, the module's GPIO pins in VDD_EXT voltage domain can only be configured to 1.8 V.

Table 14: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	14	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DATA	11	DIO	USIM1 card data	
USIM1_CLK	13	DO	USIM1 card clock	
USIM1_RST	12	DO	USIM1 card reset	
USIM1_DET	79	DI	USIM1 card hot-plug detect	It is recommended to reserve an RC circuit and pull-up resistor externally.

				If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	Share the same power supply with USIM1_VDD.
USIM2_DATA	64	DIO	USIM2 card data	If USIM2 is used, the level of GPIO pins whose voltage domain is VDD_EXT can only be configured to 1.8 V.
USIM2_CLK	62	DO	USIM2 card clock	
USIM2_RST	63	DO	USIM2 card reset	

The module supports USIM card hot-plug [6] detection via the USIM1_DET pin, and both high and low level detection are supported. The function is disabled by default. For details, please contact Quectel Technical support.

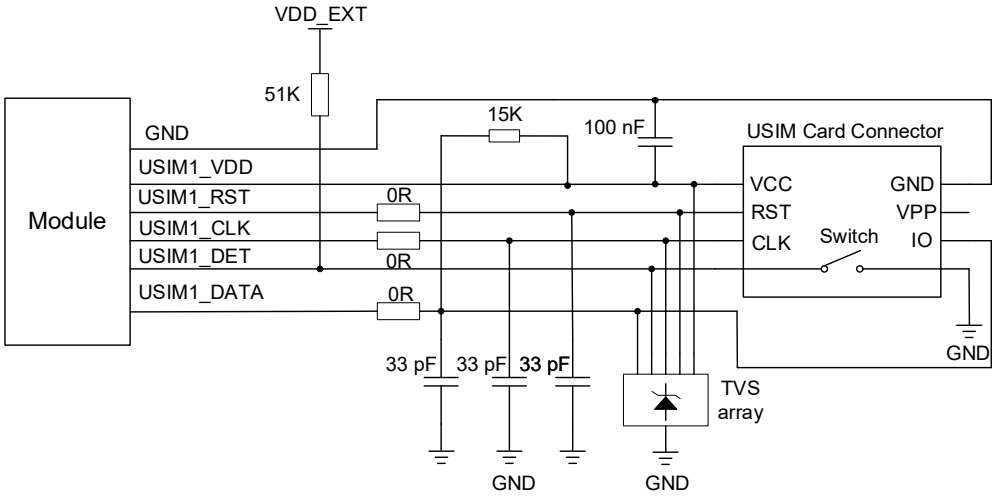
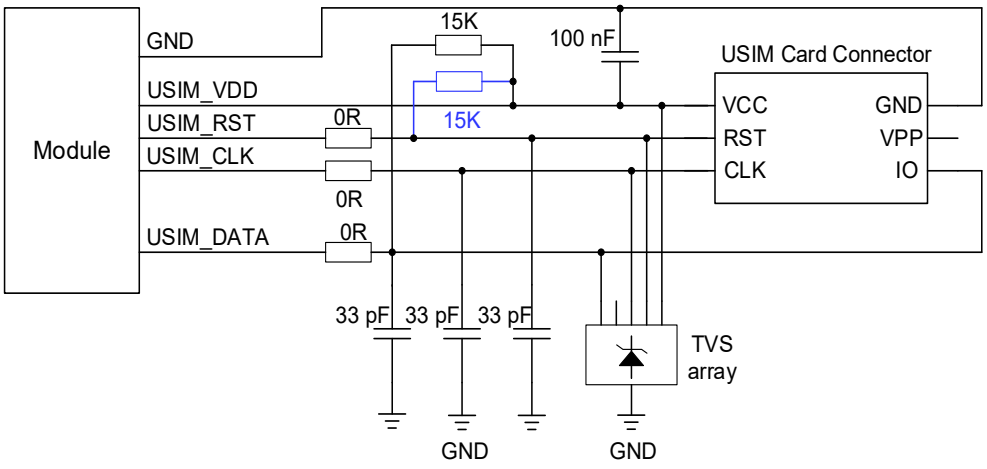


Figure 18: Reference Design of USIM1 Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, keep USIM1_DET disconnected.

[6] Only USIM1 interface supports hot-plug detect.



NOTE: Only when USIM2 is used should a 15 kΩ pull-up resistor be added to USIM2_RST.

Figure 19: Reference Design of USIM Interface with a 6-Pin USIM Card Connector

To enhance USIM card reliability and availability in applications, follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signal traces away from RF and power supply traces.
- Make sure that the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and should be placed close to the USIM card connector.
- To avoid cross talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them by surrounding them with ground.
- To improve ESD protection, it is recommended to add a TVS array on USIM pins. The parasitic capacitance of the TVS array should not exceed 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. The 33 pF capacitors on USIM_DATA, USIM_CLK and USIM_RST are used for filtering out RF interference. In addition, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the USIM card connector.
- Ensure the trace between the ground of USIM card connector and the module ground is short and wide. To maintain equal electric potential, keep the trace width for USIM_VDD at least 0.5 mm.

NOTE

The module supports Dual SIM Single Standby. USIM cards can be switched by *ql_sim_set_operate_id*. For details, please contact Quectel Technical support.

4.4. UART Interfaces

The module has 3 UART interfaces.

Table 15: UART Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART interface	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	● AT command communication, firmware upgrade and data transmission ● RTS and CTS hardware flow control
Debug UART interface	115200, 3000000, 6000000	6000000	Log output
Auxiliary UART interface	115200	115200	General-purpose UART

NOTE

The supported baud rates of UART can be configured by *ql_uart_set_dcbconfig()*. For details, see ***document [1]***.

Table 16: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	22	DO	Clear to send signal from the module	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	17	DI	Main UART receive	When the module is in sleep mode and PSM, this pin can be used for interrupt wake-up. If unused, keep it open.
MAIN_TXD	18	DO	Main UART transmit	If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit.	
AUX_RXD	28	DI	Auxiliary UART receive.	
DBG_RXD	38	DI	Debug UART receive	Test points must be

DBG_TXD	39	DO	Debug UART transmit	reserved.

If the level of the module's UART is the same as that of the MCU, and the MAIN_TXD of the module is connected to the RXD of the MCU, the MAIN_TXD should be connected to a 10 kΩ resistor and be pulled up to 1.8 V to prevent the MCU from receiving error messages when the module is in sleep mode. A voltage-level translator should be used between the module and the MCU if the level is not the same.

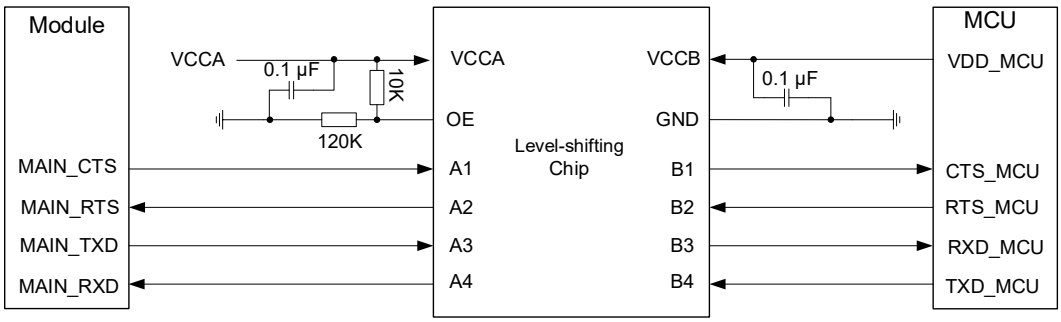


Figure 20: Reference Design of UART with a Voltage-Level Translator (Main UART)

NOTE

For this voltage-level translator, the input voltage of the power supply VCCA should be consistent with the UART level of the module, and be lower than the power supply voltage VDD_MCU connected to VCCB. In addition, to ensure the normal operation of the chip, the VCCA power supply capacity of the chip is recommended to be greater than 50 mA, and VCCA cannot be powered down when the module is in sleep mode.

Another example of level-shifting circuit is shown below. For the design of input/output circuits in dotted lines, see the ones in solid lines, but pay attention to the direction of the connection.

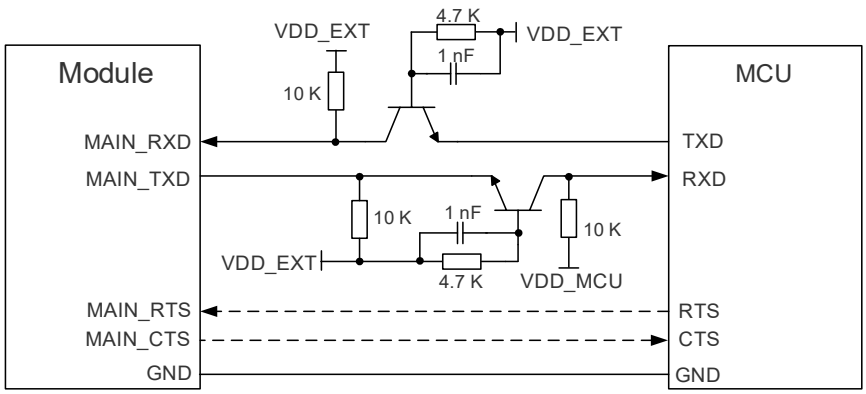


Figure 21: Reference Design of UART with Transistor Circuit (Main UART)

NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. The level-shifting circuits (***Figure 20*** and ***Figure 21***) take the main UART as an example. The circuits of the debug UART and the auxiliary UART are connected in the same way as the main UART.
4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. PCM and I2C Interfaces

The module has one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 17: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	31	DO	PCM data frame sync	If unused, keep them open.
PCM_CLK	30	DO	PCM clock	
PCM_DIN	32	DI	PCM data input	
PCM_DOUT	33	DO	PCM data output	
PCM_MCLK	26	DO	PCM main clock	

Table 18: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	67	OD	I2C serial clock	An external pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	OD	I2C serial data	

A reference design of PCM and I2C interfaces with external Codec IC is illustrated in the following figure.

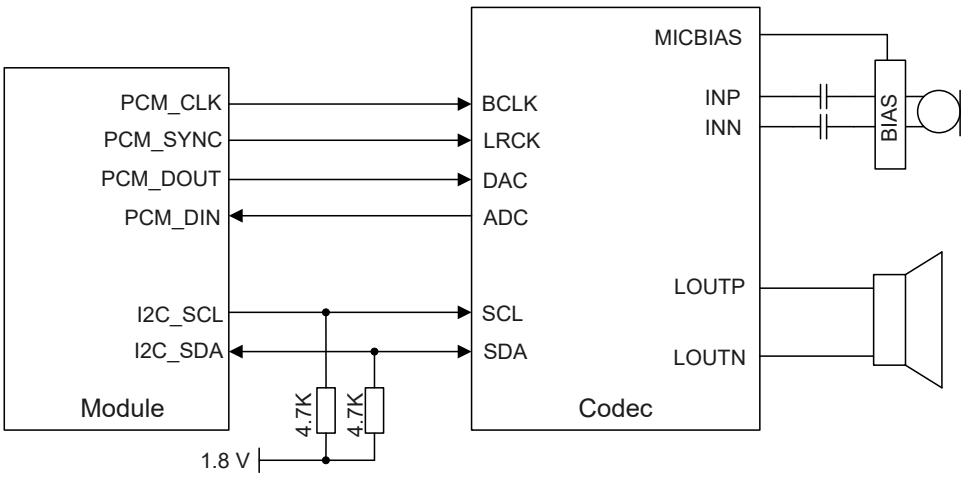


Figure 22: Reference Circuit of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve RC circuits on the PCM signal traces, especially on the PCM_CLK pin.
2. The module can only be used as a master device in applications related to both the PCM interface and the I2C interface.
3. The PCM and I2C interface level of the module should be consistent with those of the Codec chip, and the level of the pull-up power supply VDD for the module's I2C interface should be consistent with the level of its I2C interface.

4.6. PWM Audio Interface

GPIO3 and GPIO4 can be configured for PWM audio output, enabling playback functionality (recording is not supported). If the requirements for sound quality are not very high, PWM channels can be used to playback audio.

Table 19: Pin Description of PWM Audio Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO3	100	PWM0	DO	Audio output (+)	It is recommended to use these pins as the PWM audio output pins. If unused, keep them open.
GPIO4	101	PWM0n	DO	Audio output (-)	

The reference design is as follows:

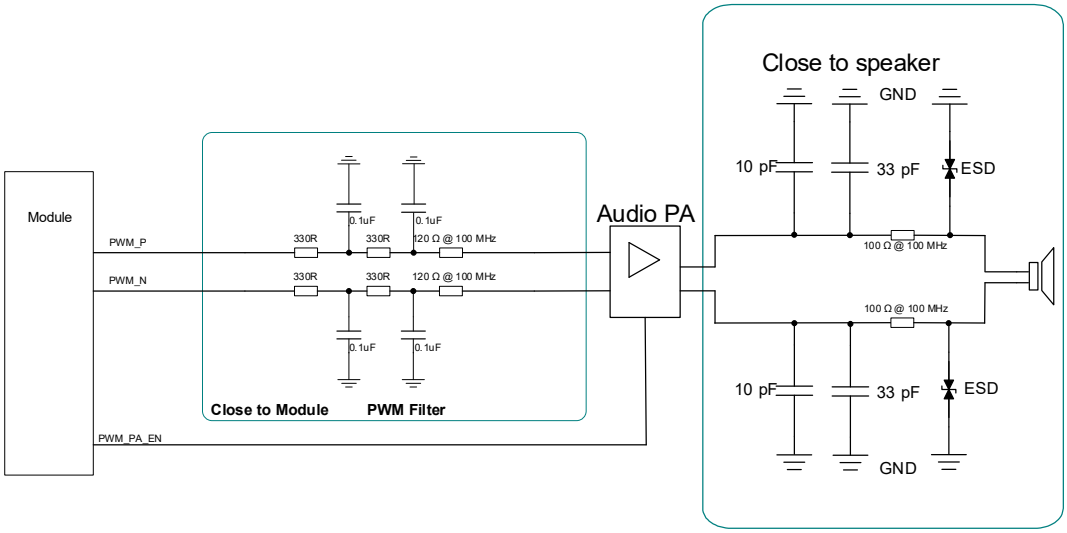


Figure 23: Reference Circuit of PWM Interface

NOTE

1. It is recommended to configure pins 100 and 101 as PWM audio output, which supports single-ended or differential modes. For details, please contact Quectel technical support.
2. Reserve pin 26 (PCM_MCLK) as the PA enable signal pin and keep it open if it is unused. Other GPIOs can also be used as PA enable pins. For details, please contact Quectel technical support.

4.7. ADC Interfaces

The module has two Analog-to-Digital Converter (ADC) interfaces. To improve the voltage measurement accuracy, the trace of ADC interface should be surrounded by ground.

Table 20: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI	General-purpose ADC interface	

Table 21: ADC Interface Features

Name	Min.	Typ.	Max.	Unit
ADC0 input voltage range	0	-	1.6	V
ADC1 input voltage range	0	-	1.6	V
ADC resolution	-	12	-	bits

You can execute *ql_adc_get_volt()* to read the ADC interface voltage. The relation between *ql_adc_channel_id* and ADC channel is as follows. For more details about the API, see ***document [8]***.

Table 22: Relation between *ql_adc_channel_id* and ADC channel

ql_adc_channel_id	ADC channel
QL_ADC0_CHANNEL	ADC0
QL_ADC1_CHANNEL	ADC1

NOTE

1. The input voltage range of ADC0 and ADC1 interfaces is 0–1.6 V. Please note that the effective input voltage range of ADC interfaces is 0.1–1.5 V. There may be relatively large errors in the ranges of 0–0.1 V and 1.5–1.6 V, and it is not recommended to use the ADC interfaces within these ranges.
2. When the collected voltage is greater than or equal to 1.5 V, it is recommended to use the resistor divider circuit for ADC application. The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.

4.8. LCM interface

The module supports LCM interface.

Table 23: Pin Description of LCM interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	If unused, keep them open.
LCD_SPI_DOUT	50	DO	LCD SPI data output	
LCD_SPI_RS	51	DO	LCD SPI register select	
LCD_SPI_CS	52	DO	LCD SPI chip select	
LCD_SPI_CLK	53	DO	LCD SPI clock	
LCD_TE	78	DI	LCD tearing effect	

NOTE

For LCM interface signals, it is recommended to reserve termination resistors and filter capacitors, and their resistance and capacitance values should be adjusted according to actual debugging conditions.

4.9. Camera interface

The module has one camera interface supporting cameras up to 0.3 MP.

Table 24: Pin Description of LCM interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	54	DO	Camera master clock	If unused, keep them open.
CAM_SPI_DATA0	55	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	56	DI	Camera SPI data bit 1	
CAM_SPI_CLK	80	DO	Camera SPI clock	
CAM_PWDN	81	DO	Camera power down	
CAM_RST	103	DO	Camera reset	
CAM_I2C_SCL	57	OD	Camera I2C clock	An external pull-up resistor is required. If unused, keep them open.
CAM_I2C_SDA	58	OD	Camera I2C data	

NOTE

It is recommended to reserve termination resistors and filter capacitors for the above clock and data pins, and their resistance and capacitance values should be adjusted according to actual debugging conditions.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface and Frequency Bands

Table 25: Pin Description of Cellular/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	Main antenna/Wi-Fi Scan antenna interface	50 Ω impedance.

NOTE

1. The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.
2. Main antenna and Wi-Fi Scan antenna only support passive antennas.

Table 26: Operating Frequency of EG800Z-CN (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894

LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

EG800Z-CN B41 only supports 140 MHz (2535–2675 MHz).

Table 27: Operating Frequency of EG800Z-EU (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

Table 28: Operating Frequency of EG800Z-LA (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2698
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180

Table 29: Operating Frequency of EG800Z-GL (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2698
LTE-FDD B8	880–915	925–960
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B14	788–798	758–768
LTE-FDD B17	704–716	734–746
LTE-FDD B18	815–830	860–875
LTE-FDD B19	830–845	875–890

LTE-FDD B20	832–862	791–821
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–849	859–894
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-FDD B71	663–698	617–652
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

5.1.2. Transmit Power

Table 30: Transmit Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE bands	23 dBm ±2 dB	< -39 dBm

NOTE

The module supports the above transmit power in hardware, but actual applications may be subject to local regulations.

5.1.3. Receiver Sensitivity

Table 31: EG800Z-CN Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B1 (10 MHz)	-98.0	-93.3

LTE-FDD B3 (10 MHz)	-98.0	-90.3
LTE-FDD B5 (10 MHz)	-98.0	-91.8
LTE-FDD B8 (10 MHz)	-98.0	-90.8
LTE-TDD B34 (10 MHz)	-99.5	-93.8
LTE-TDD B38 (10 MHz)	-99.0	-93.3
LTE-TDD B39 (10 MHz)	-99.5	-93.8
LTE-TDD B40 (10 MHz)	-99.0	-93.8
LTE-TDD B41 (10 MHz)	-98.5	-91.8

Table 32: EG800Z-EU Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B1 (10 MHz)	-98.0	-93.3
LTE-FDD B3 (10 MHz)	-98.5	-90.3
LTE-FDD B5 (10 MHz)	-99.0	-91.8
LTE-FDD B7 (10 MHz)	-96.5	-91.3
LTE-FDD B8 (10 MHz)	-99.0	-90.8
LTE-FDD B20 (10 MHz)	-99.0	-90.8
LTE-FDD B28 (10 MHz)	-99.0	-92.3
LTE-TDD B38 (10 MHz)	-98.0	-93.3
LTE-TDD B40 (10 MHz)	-98.5	-93.8
LTE-TDD B41 (10 MHz)	-98.0	-91.8

Table 33: EG800Z-LA Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B2 (10 MHz)	-97.5	-91.3
LTE-FDD B3 (10 MHz)	-98	-90.3
LTE-FDD B4 (10 MHz)	-98.5	-93.3
LTE-FDD B5 (10 MHz)	-98	-91.8
LTE-FDD B7 (10 MHz)	-96.5	-91.3
LTE-FDD B8 (10 MHz)	-98.5	-90.8
LTE-FDD B28 (10 MHz)	-98.5	-92.3
LTE-FDD B66 (10 MHz)	-98.5	-92.8

Table 34: EG800Z-GL Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B1 (10 MHz)	-97.5	-93.3
LTE-FDD B2 (10 MHz)	-98	-91.3
LTE-FDD B3 (10 MHz)	-98	-90.3
LTE-FDD B4 (10 MHz)	-97.5	-93.3
LTE-FDD B5 (10 MHz)	-98	-91.8
LTE-FDD B7 (10 MHz)	-96	-91.3
LTE-FDD B8 (10 MHz)	-98.5	-90.8
LTE-FDD B12 (10 MHz)	-97	-91
LTE-FDD B13 (10 MHz)	-98	-91
LTE-FDD B14 (10 MHz)	-98	-91
LTE-FDD B17 (10 MHz)	-97	-91

LTE-FDD B18 (10 MHz)	-98	-94.5
LTE-FDD B19 (10 MHz)	-98	-94.5
LTE-FDD B20 (10 MHz)	-98	-90.8
LTE-FDD B25 (10 MHz)	-97.5	-91.3
LTE-FDD B26 (10 MHz)	-98	-92.0
LTE-FDD B28 (10 MHz)	-98	-92.3
LTE-FDD B66 (10 MHz)	-97.5	-92.8
LTE-FDD B71 (10 MHz)	-97	-93.3
LTE-TDD B34 (10 MHz)	-98.5	-93.8
LTE-TDD B38 (10 MHz)	-97.5	-93.3
LTE-TDD B39 (10 MHz)	-98.5	-93.8
LTE-TDD B40 (10 MHz)	-98.5	-93.8
LTE-TDD B41 (10 MHz)	-97.5	-91.8

5.1.4. Reference Design

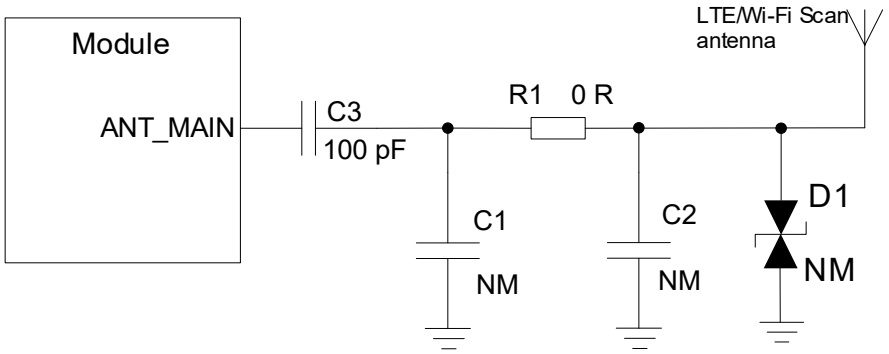


Figure 24: Reference Design of RF Antenna Interfaces

NOTE

1. Place the dual L-type components (C3, C1, R1 and C2) to antennas as close as possible. Capacitors C1 and C2 are not mounted by default.
2. Notes on C3:

1) If there is DC power at the antenna ports, place a capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
2) If there is no DC power in the peripheral design:
   a) Do not reserve C3.
   b) If C3 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor. You can also match the component according to the debugging results.

3. It is recommended to reserve an ESD protection component for the antenna interface to effectively prevent static electricity and the junction capacitance should not exceed 0.05 pF.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

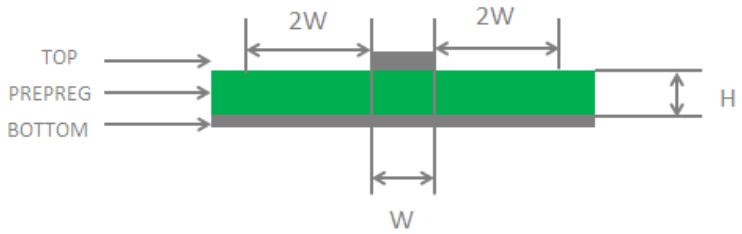


Figure 25: Microstrip Design on a 2-layer PCB

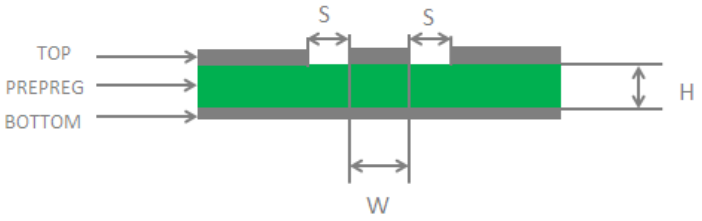


Figure 26: Coplanar Waveguide Design on a 2-layer PCB

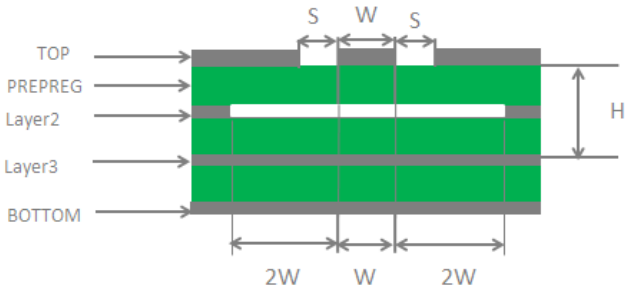


Figure 27: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

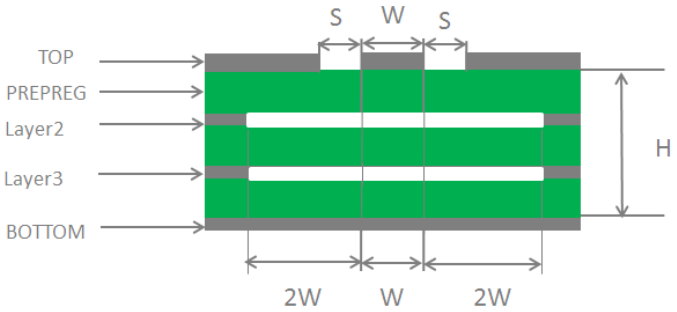


Figure 28: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [9]***.

5.3. Requirements for Antenna Design

Table 35: Antenna Design Requirements

Antenna Type	Requirements
Cellular/Wi-Fi Scan	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

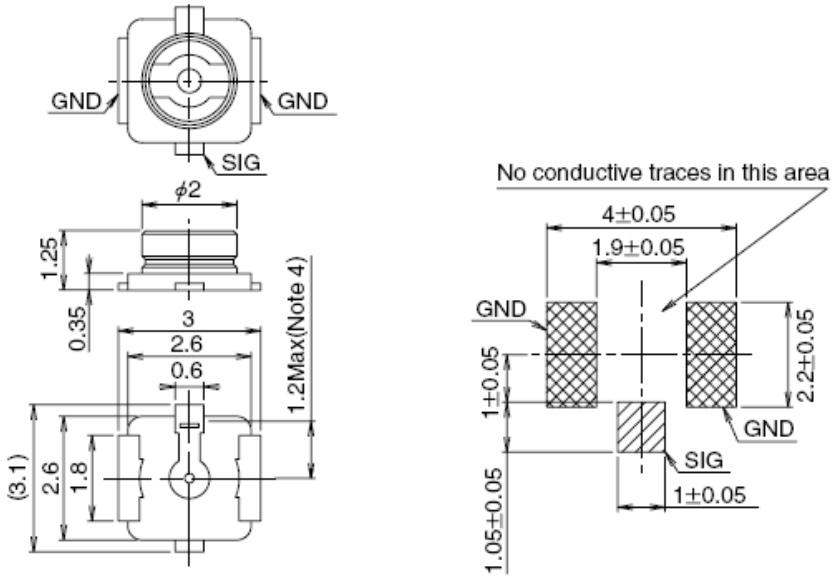


Figure 29: Receptacle Dimensions (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

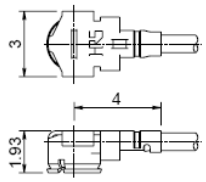
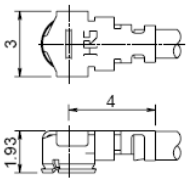
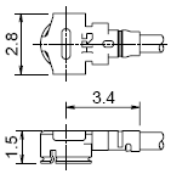
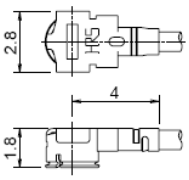
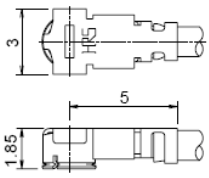
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 30: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

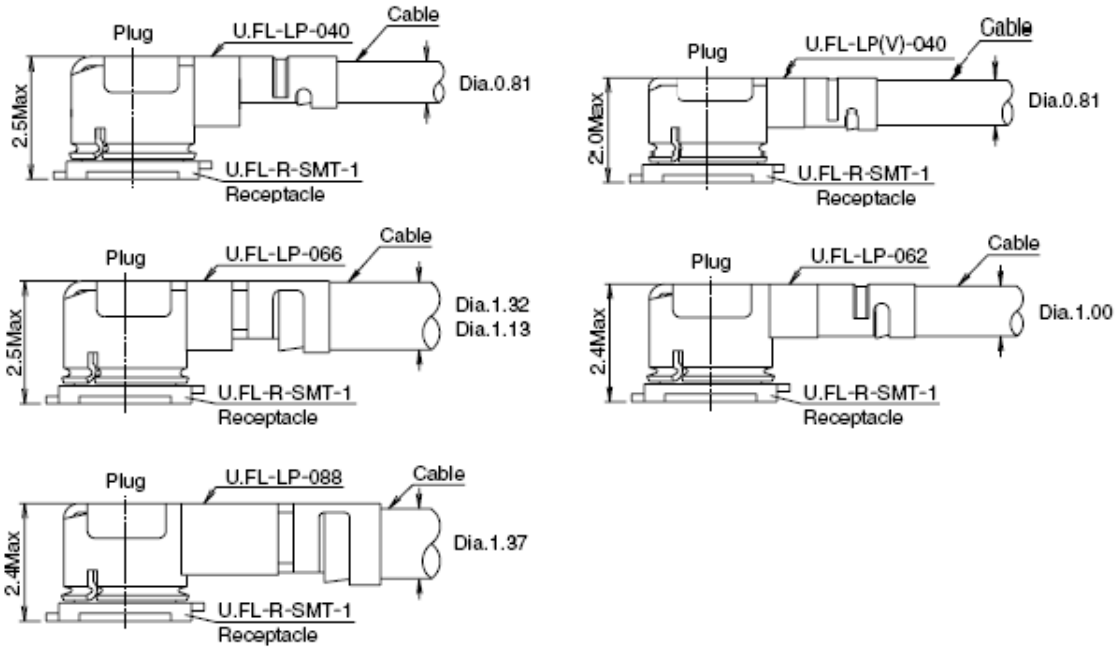


Figure 31: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	-0.3	5	V
Voltage at USB_VBUS	-0.3	5.25	V
Voltage at digital pins	-0.3	3.6	V

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

6.2. Power Supply Ratings

Table 37: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak supply current under BB and RF	At maximum power control level	-	-	1.2	A

	application scenarios					
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 38: EG800Z-CN Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	Enter PSM	4.11	μA
Sleep	Minimum functionality mode (USB disconnected)	0.05	mA
	Airplane mode (USB disconnected)	0.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	0.97	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.63	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.44	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.34	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.06	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.56	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.36	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.3	mA
Idle	LTE-FDD @ PF = 64 (USB disconnected)	4.22	mA
	LTE-FDD @ PF = 64 (USB connected)	27.06	mA
	LTE-TDD @ PF = 64 (USB disconnected)	4.28	mA
	LTE-TDD @ PF = 64 (USB connected)	27.4	mA
LTE data transmission	LTE-FDD B1	500	mA
	LTE-FDD B3	480	mA

	LTE-FDD B5	490	mA
	LTE-FDD B8	550	mA
	LTE-TDD B34	180	mA
	LTE-TDD B38	180	mA
	LTE-TDD B39	180	mA
	LTE-TDD B40	180	mA
	LTE-TDD B41 (140 MHz)	200	mA

Table 39: EG800Z-EU Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	Enter PSM	4.11	μA
Sleep	Minimum functionality mode (USB disconnected)	0.05	mA
	Airplane mode (USB disconnected)	0.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	0.94	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.61	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.41	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.30	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.11	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.72	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.5	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.29	mA
Idle	LTE-FDD @ PF = 64 (USB disconnected)	3.15	mA
	LTE-FDD @ PF = 64 (USB connected)	25.98	mA
	LTE-TDD @ PF = 64 (USB disconnected)	3.88	mA
	LTE-TDD @ PF = 64 (USB connected)	26.73	mA

LTE data transmission	LTE-FDD B1	500	mA
	LTE-FDD B3	550	mA
	LTE-FDD B5	480	mA
	LTE-FDD B7	560	mA
	LTE-FDD B8	480	mA
	LTE-FDD B20	440	mA
	LTE-FDD B28	480	mA
	LTE-TDD B38	170	mA
	LTE-TDD B40	170	mA
	LTE-TDD B41 (194 MHz)	170	mA

Table 40: EG800Z-LA Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	Enter PSM	2.91	μA
Sleep	Minimum functionality mode (USB disconnected)	0.6	mA
	Airplane mode (USB disconnected)	0.6	mA
	LTE-FDD @ PF = 32（USB disconnected）	1.06	mA
	LTE-FDD @ PF = 64（USB disconnected）	0.56	mA
	LTE-FDD @ PF = 128（USB disconnected）	0.36	mA
	LTE-FDD @ PF = 256（USB disconnected）	0.30	mA
Idle	LTE-FDD @ PF = 64（USB disconnected）	3.60	mA
	LTE-FDD @ PF = 64（USB connected）	26.68	mA
LTE data transmission	LTE-FDD B2	520	mA
	LTE-FDD B3	540	mA
	LTE-FDD B4	500	mA

	LTE-FDD B5	490	mA
	LTE-FDD B7	560	mA
	LTE-FDD B8	480	mA
	LTE-FDD B28	480	mA
	LTE-FDD B66	510	mA

Table 41: EG800Z-GL Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.88	μA
PSM	Enter PSM	3.4	μA
Sleep	Minimum functionality mode (USB disconnected)	0.05	mA
	Airplane mode (USB disconnected)	0.84	mA
	LTE-FDD @ PF = 32（USB disconnected）	1.83	mA
	LTE-FDD @ PF = 64（USB disconnected）	1.28	mA
	LTE-FDD @ PF = 128（USB disconnected）	1.44	mA
	LTE-FDD @ PF = 256（USB disconnected）	1.07	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.93	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.32	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.14	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.98	mA
Idle	LTE-FDD @ PF = 64（USB disconnected）	6.36	mA
	LTE-FDD @ PF = 64（USB connected）	26.74	mA
	LTE-TDD @ PF = 64 (USB disconnected)	6.30	mA
	LTE-TDD @ PF = 64 (USB connected)	26.78	mA
LTE data	LTE-FDD B1	550	mA

transmission	LTE-FDD B2	500	mA
	LTE-FDD B3	530	mA
	LTE-FDD B4	550	mA
	LTE-FDD B5	550	mA
	LTE-FDD B7	550	mA
	LTE-FDD B8	630	mA
	LTE-FDD B12	560	mA
	LTE-FDD B13	580	mA
	LTE-FDD B14	550	mA
	LTE-FDD B17	560	mA
	LTE-FDD B18	550	mA
	LTE-FDD B19	550	mA
	LTE-FDD B20	510	mA
	LTE-FDD B25	500	mA
	LTE-FDD B26	550	mA
	LTE-FDD B28	570	mA
	LTE-FDD B66	550	mA
	LTE-FDD B71	530	mA
	LTE-TDD B34	180	mA
	LTE-TDD B38	180	mA
	LTE-TDD B39	180	mA
	LTE-TDD B40	180	mA
	LTE-TDD B41	180	mA

NOTE

The above power consumption data are tested under 50 Ω impedance.

6.4. Digital I/O Characteristics

Table 42: VDD_EXT I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT + 0.3
V_{IL}	Low-level input voltage	-0.3	0.2 × VDD_EXT
V_{OH}	High-level output voltage	0.8 × VDD_EXT	-
V_{OL}	Low-level output voltage	-	0.15 × VDD_EXT

Table 43: USIM Low/High-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × USIM_VDD	-
V_{IL}	Low-level input voltage	-	0.2 × USIM_VDD
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-
V_{OL}	Low-level output voltage	-	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 44: Electrostatics Discharge Characteristics (Temperature: 15–35 °C, Humidity: 30–60 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 45: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Normal operating temperature [7]	-35	+25	+75	°C
Extended operating temperature [8]	-40	-	+85	°C
Storage temperature	-40	-	+90	°C

[7] Within this range, the module's indicators comply with 3GPP specification requirements.
[8] Within the range of -40 to -35 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

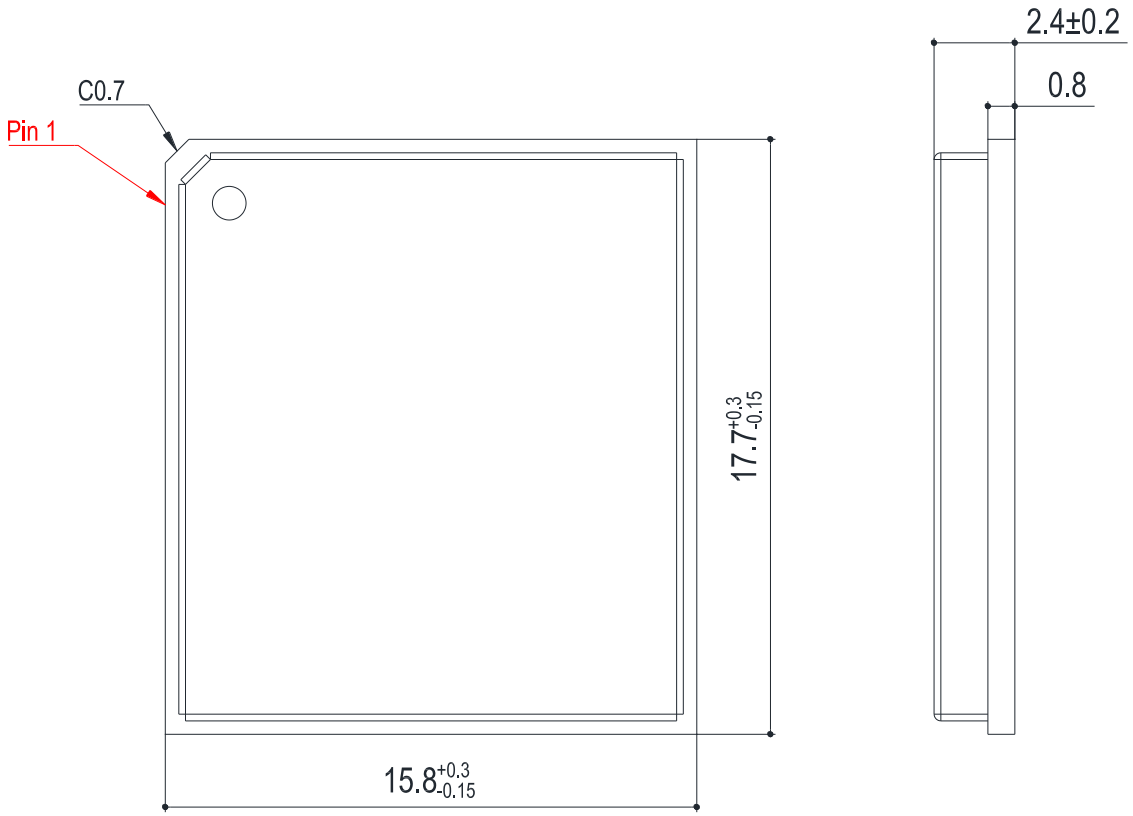


Figure 32: Module Top and Side Dimensions (Unit: mm)

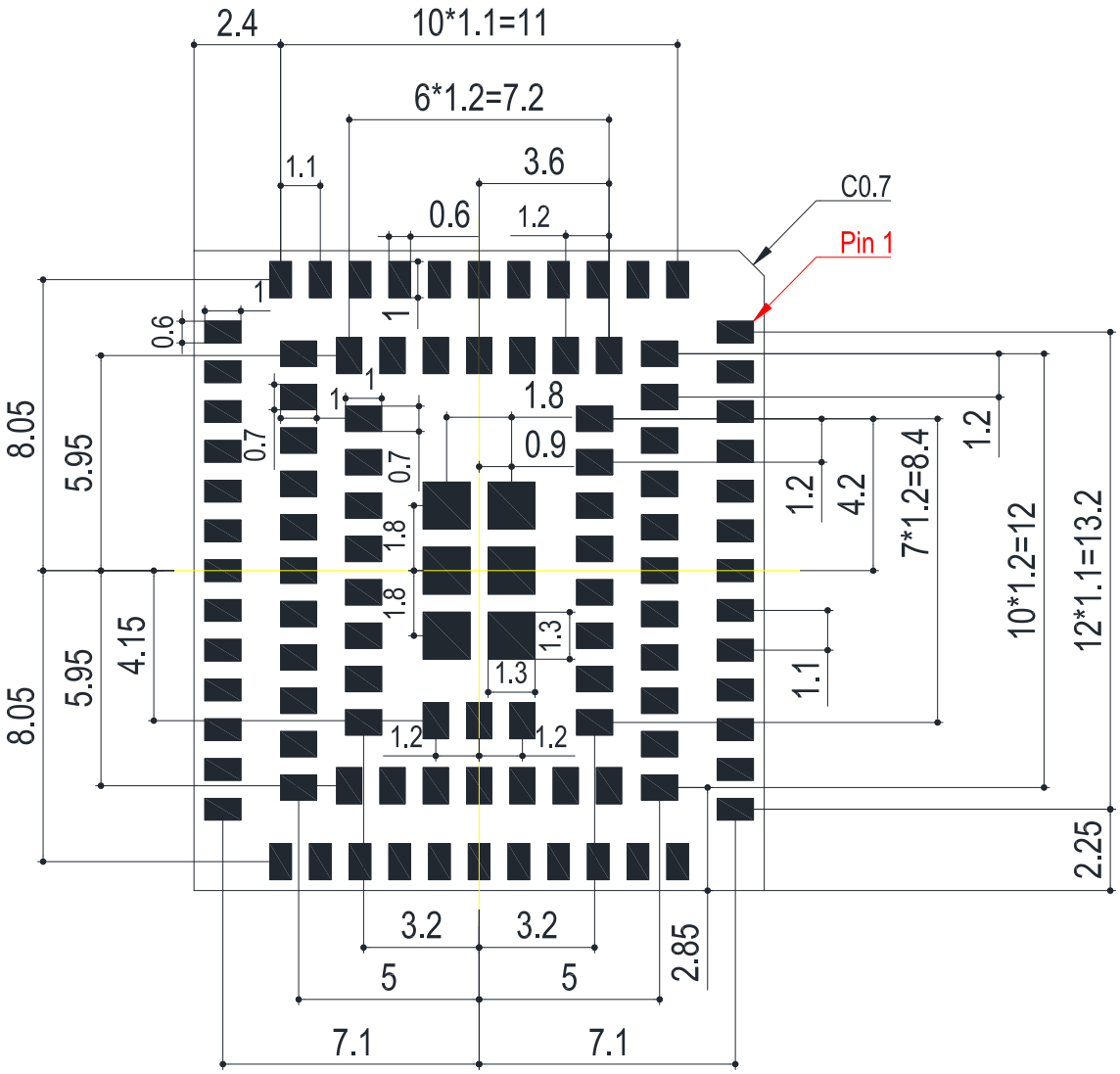


Figure 33: Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

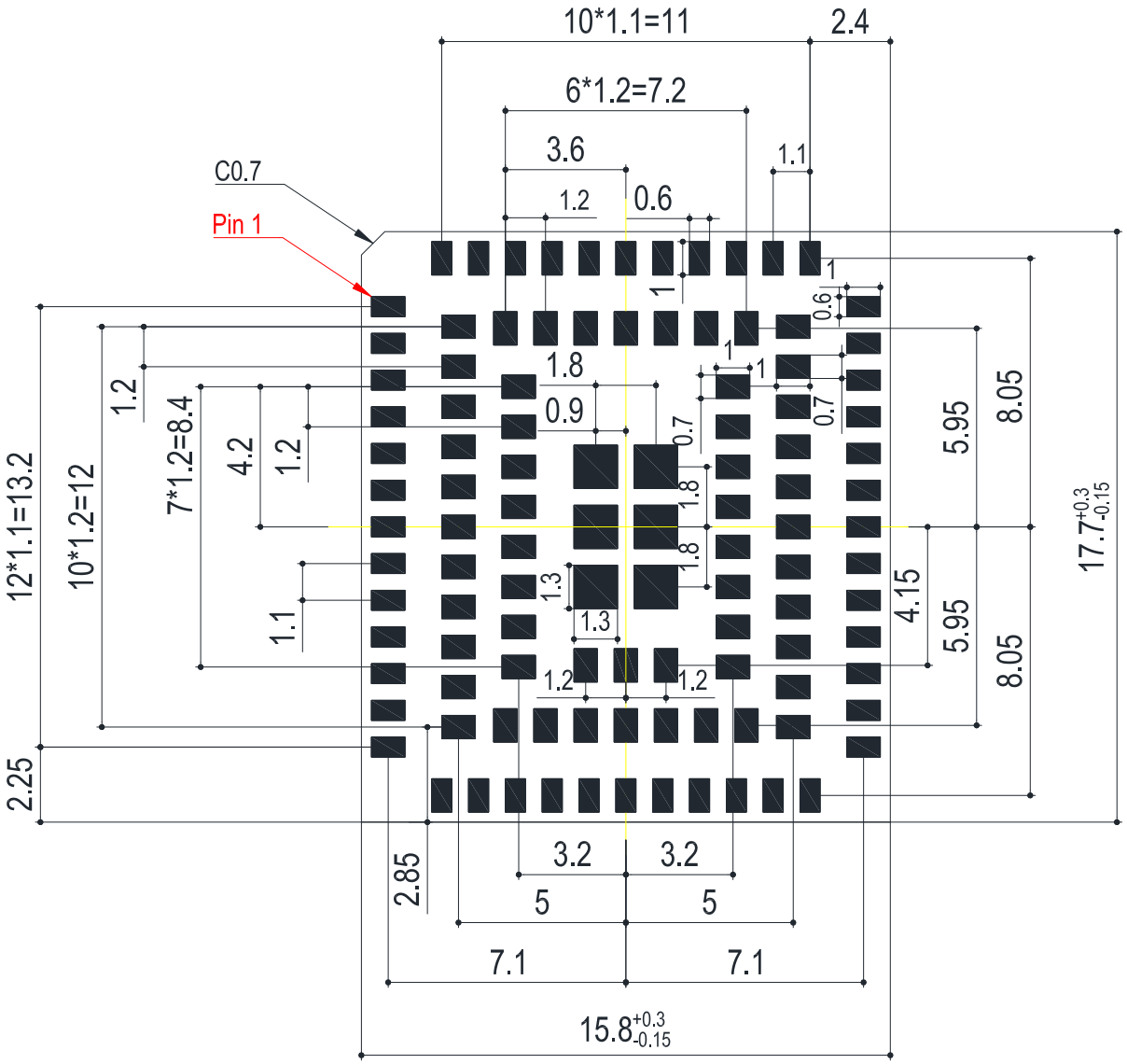


Figure 34: Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

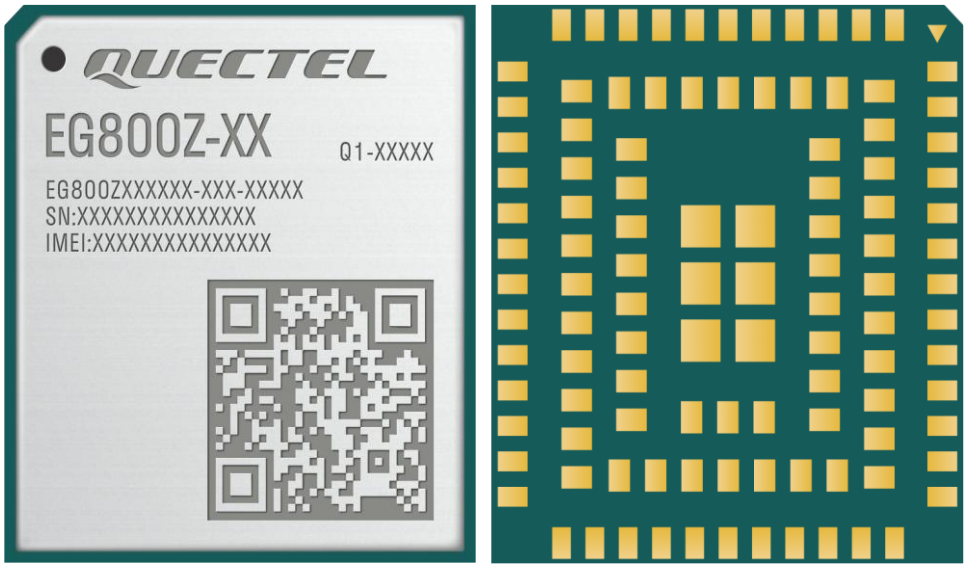


Figure 35: Module Top and Bottom Views

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [10]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

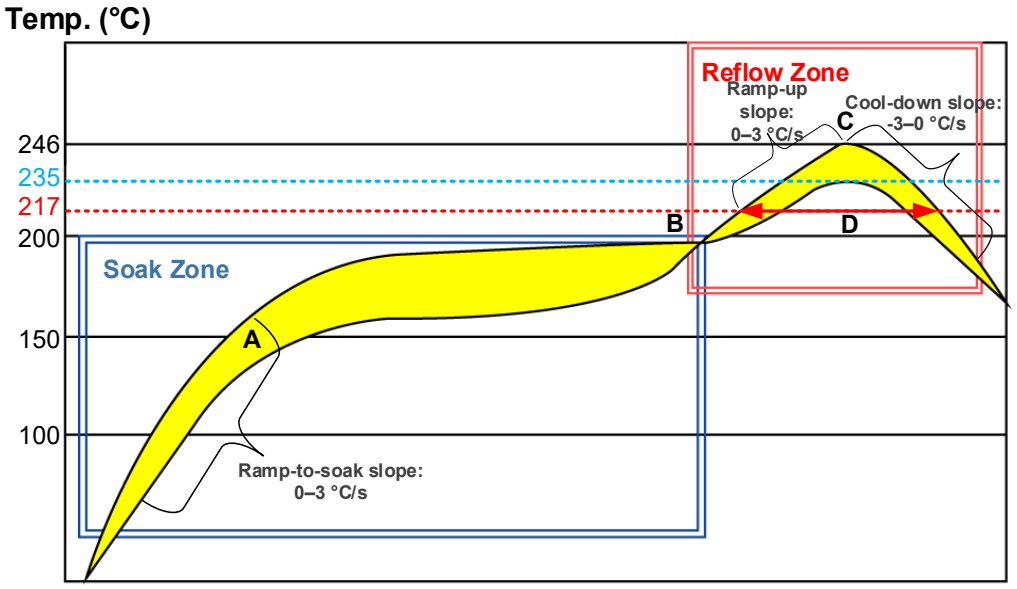


Figure 36: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic

soldering) that is not mentioned in ***document [11]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

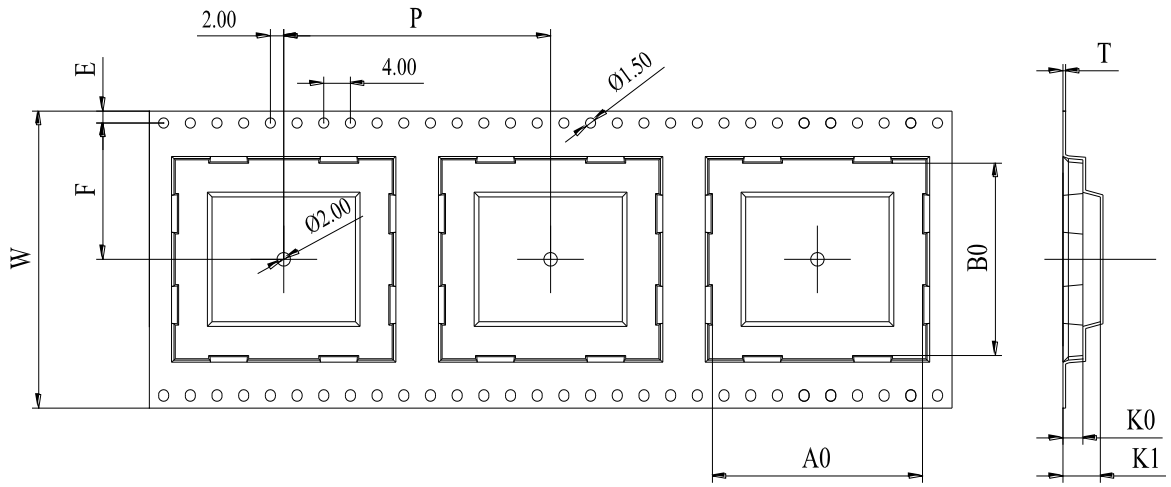


Figure 37: Carrier Tape Dimension Drawing (Unit: mm)

Table 47: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	4.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

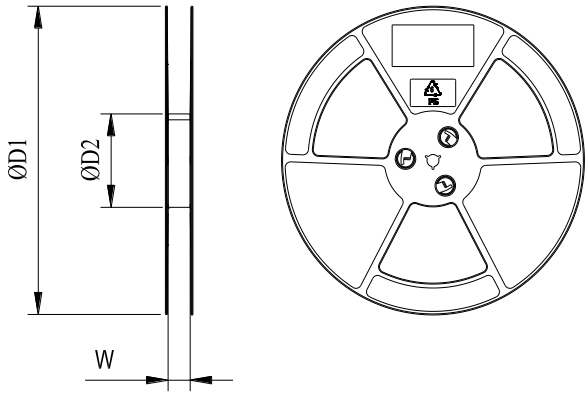


Figure 38: Plastic Reel Dimension Drawing

Table 48: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

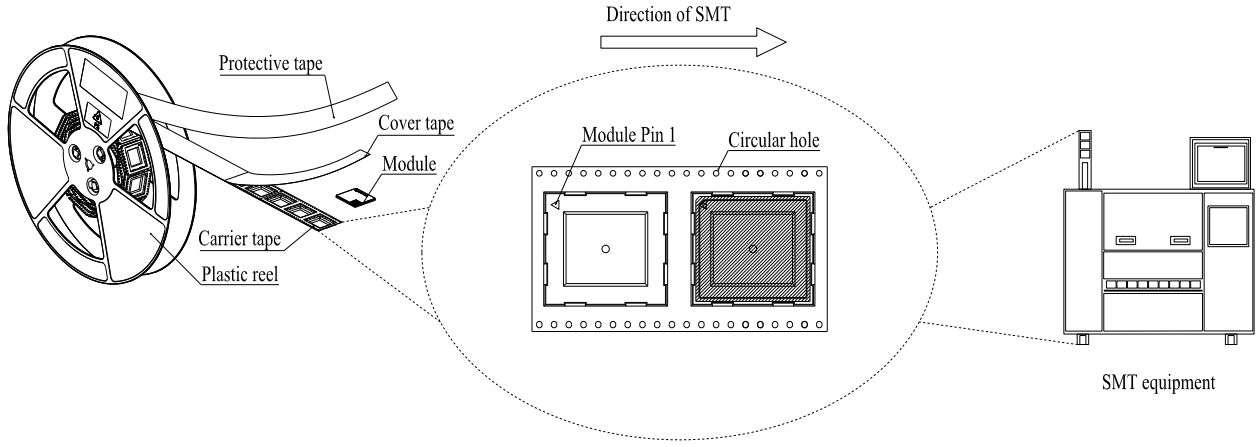
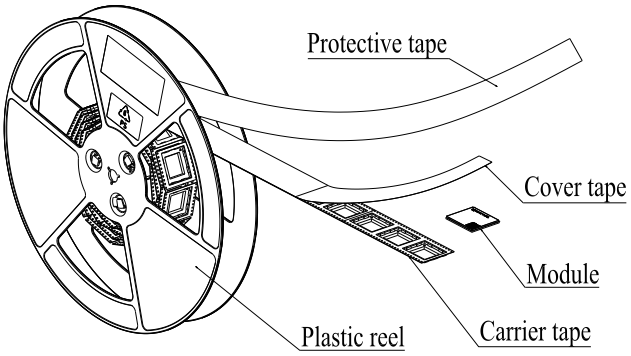


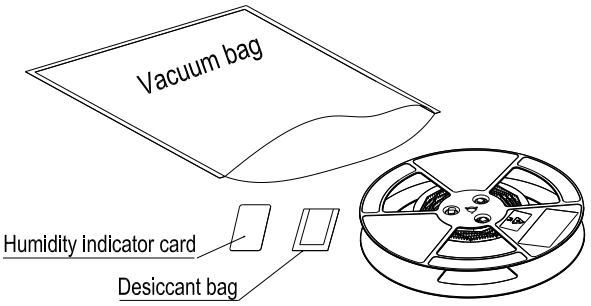
Figure 39: Mounting Direction

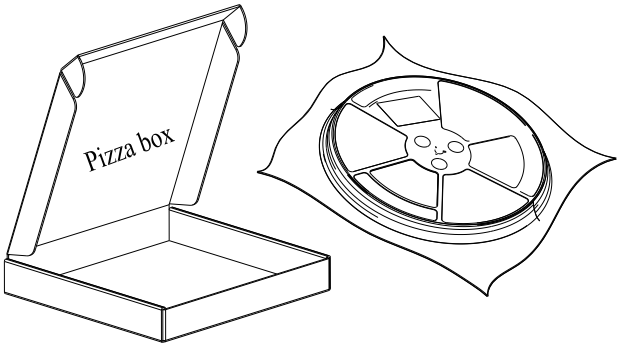
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

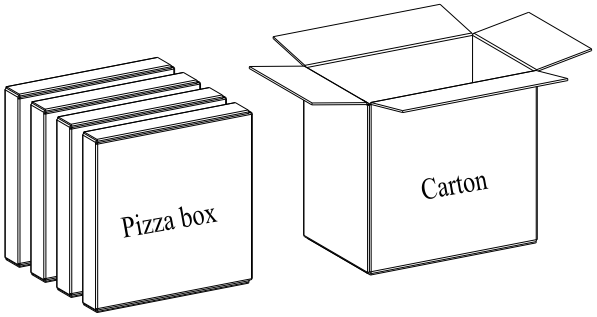


Figure 40: Packaging Process

9 Appendix References

Table 49: Related Documents

Document Name
[1] Quectel_EG800Z_Series_QuecOpen_UART_Management_Guide
[2] Quectel_EG800Z_Series_QuecOpen(SDK)_GPIO_Configuration
[3] Quectel_LTE_OPEN_EVB_User_Guide
[4] Quectel_EG800Z_Series_QuecOpen(SDK)_Device_Management_Guide
[5] Quectel_EG800Z_Series_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[6] Quectel_EG800Z_Series_QuecOpen(SDK)_PSM_Development_Guide
[7] Quectel_EG800Z_Series_QuecOpen(SDK)_Booting&Shutdown_Development_Guide
[8] Quectel_EG800Z_Series_QuecOpen(SDK)_ADC_Develpment_Guide
[9] Quectel_RF_Layout_Application_Note
[10] Quectel_Module_Stencil_Design_Requirements
[11] Quectel_Module_SMT_Application_Note

Table 50: Terms and Abbreviations

Abbreviation	Description
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CTS	Clear To Send
DRX	Discontinuous Reception

DSSS	Direct Sequence Spread Spectrum
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GND	Ground
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
VSWR	Voltage Standing Wave Ratio