

EC800K&EG800K Series QuecOpen

Reference Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2023-10-20	Kelly WANG/ Stefan FAN	Creation of the document
1.0	2024-01-16	Kelly WANG/ Stefan FAN	First official release
1.1	2024-07-30	Reuben WANG/ Stefan FAN	<ol style="list-style-type: none"> Added the applicable module EG800K-LA. Added a 100 pF capacitor in the LTE/Wi-Fi Scan antenna design (Sheet 9).
1.2	2025-02-26	Reuben WANG/ Kevin SU	<ol style="list-style-type: none"> Deleted the description specifying Wi-Fi scan function is optional. Updated the power supply for the module from 2.0 A to 1.5 A (Sheets 1 & 2 & 5). Added the circuit of Wi-Fi module (FGM842D series) design (Sheets 1 & 2 & 3 & 5 & 17). Updated the direction of SPK_P and SPK_N signal traces in TM8211 circuit design (Sheet 14).

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1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC800K-CN and EG800K series (comprising EG800K-CN, EG800K-EU and EG800K-LA) modules in QuecOpen® solution, including block diagram, power system block diagram, module interfaces, MCU interfaces, power supply design, USIM interface, UART interface and Wi-Fi module design.

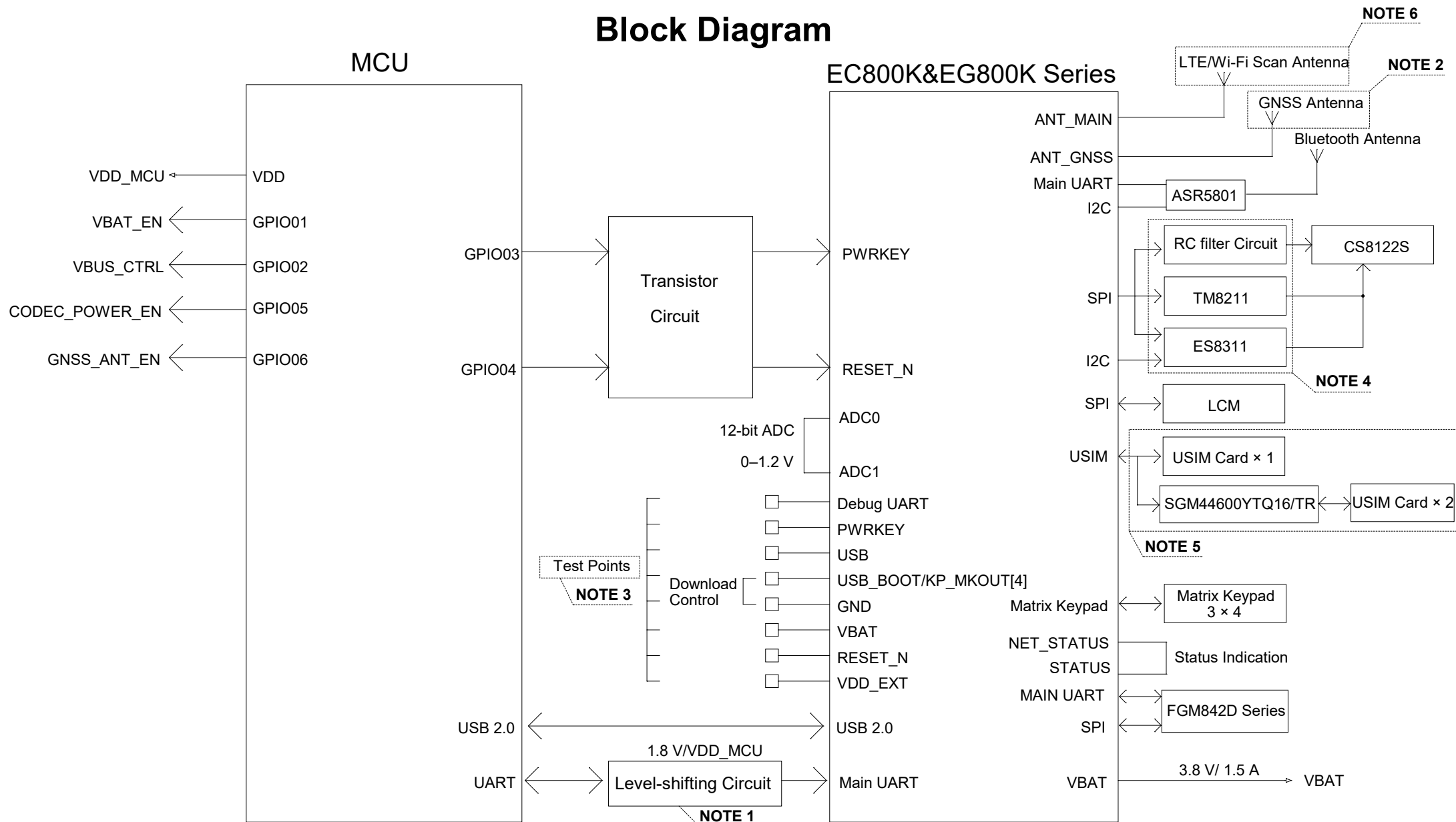
1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.

2. Only EG800K-CN supports GNSS function.

3. Test points must be reserved for DBG_TXD/RXD, USB_DP/DM and USB_VBUS.

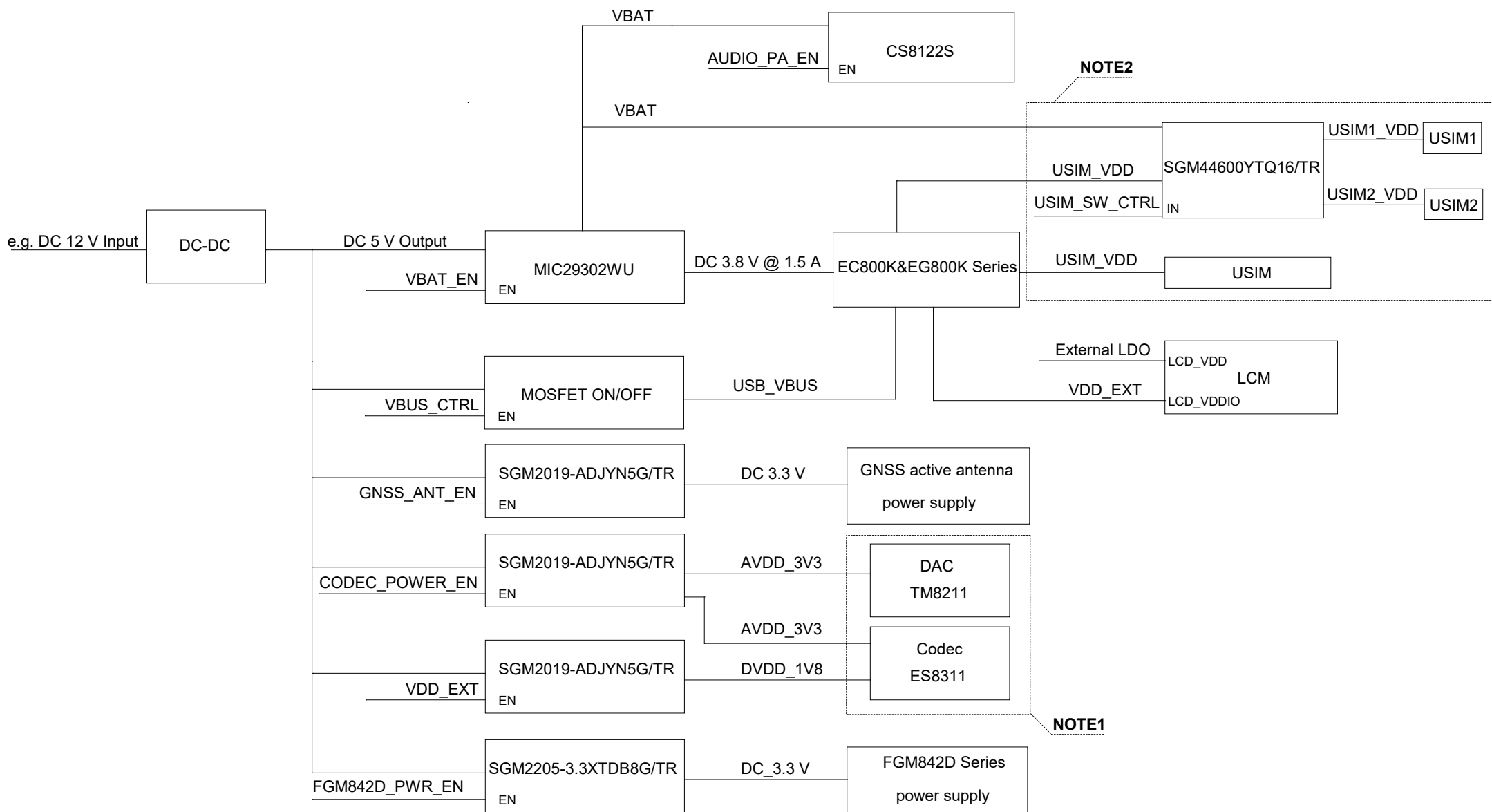
It is recommended to reserve test points for VDD_EXT, USB_BOOT, PWRKEY and VBAT. If RESET_N is unused, it is recommended to reserve a test point.

4. RC filter circuit design is used by default, and TM8211 or ES8311 circuit design can be selected externally for higher audio requirements.

5. The module supports single USIM card interface by default. If dual USIM card function is required, an analog switch must be added for your design.

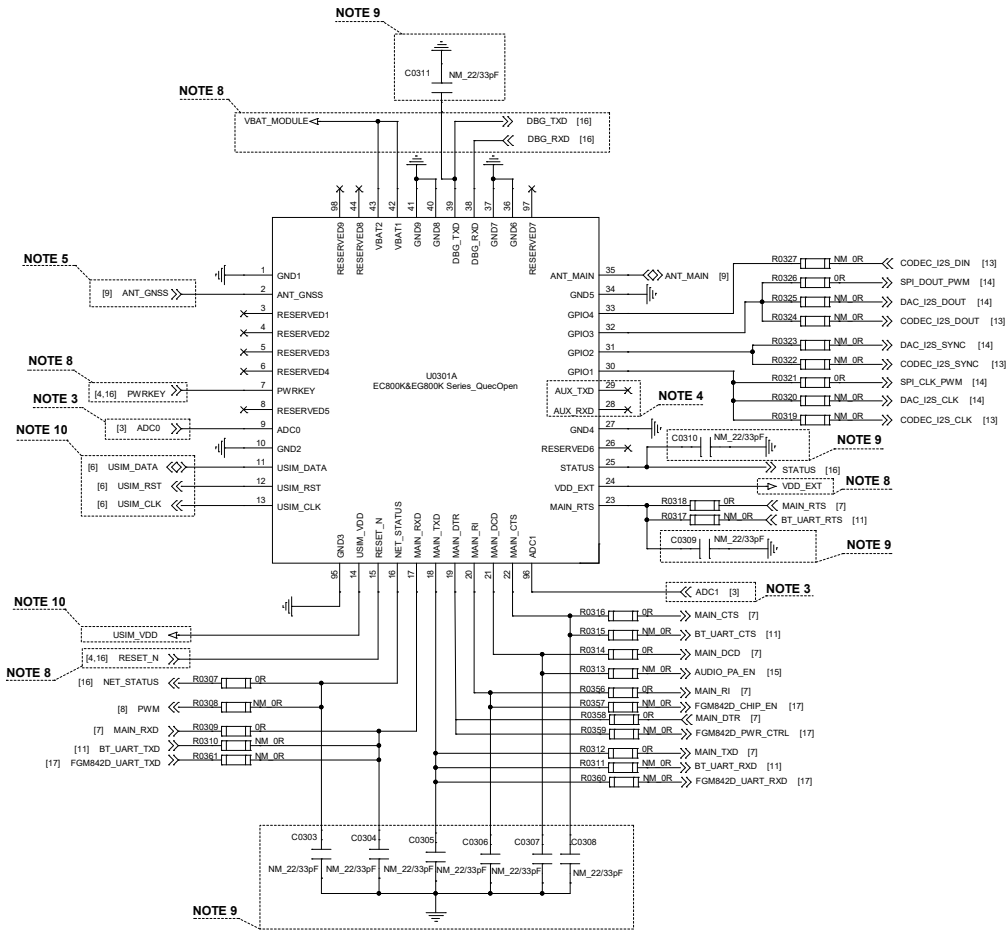
6. Wi-Fi Scan function shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.

Power System Block Diagram



- NOTE:**
1. RC filter circuit design is used by default, and TM8211 or ES8311 circuit design can be selected externally for higher audio requirements.
 2. The module supports single USIM card interface by default. If dual USIM card function is required, an analog switch must be added for your design, and the module does not support USIM card hot-plug detect function in such case.

Module Interfaces

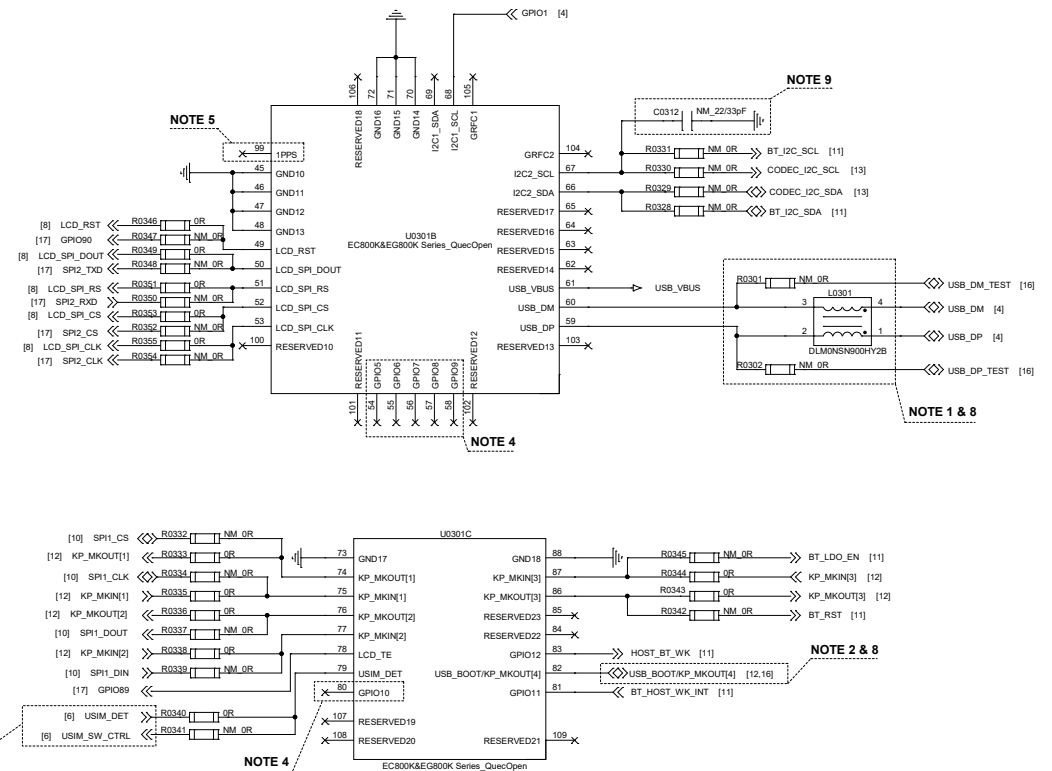


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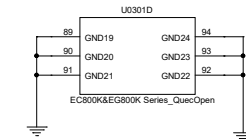
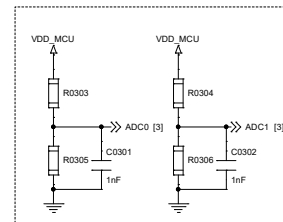
1. It is recommended to add a common mod choke L0301 in series between the module and your MCU to suppress EMI.
Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.

Place L0301 and two resistors R0301 and R0302, close to the module to ensure USB signal integrity.
2. USB_BOOT/KP_MKOUT[4] cannot be pulled down to low level before the module starts up successfully. Otherwise, the module will enter forced download mode when it starts up.
3. The input voltage range of ADC0 and ADC1 is 0–1.2 V. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 voltage inputs respectively, and the required resistance of the two resistors (R0304 and R0306) that connected to VDD_MCU is between 100 kΩ and 1 MΩ. The accuracy of the resistors directly affects ADC sampling error. It is recommended to use resistors with 1 % accuracy. For higher ADC accuracy, resistors with 0.5 % accuracy are recommended.
4. For EG800K-CN, pins 28, 29, 54–58 and 80 are RESERVED, and they should be kept open.
5. Only EG800K-CN supports GNSS function.
6. Connect all GND pins to ground, and keep unused and RESERVED pins open.
7. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer.
Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.
8. Test points must be reserved for DBG_TXD/RXD, USB_DP/DM and USB_VBUS.
It is recommended to reserve test points for VDD_EXT, USB_BOOT/KP_MKOUT[4], PWRKEY and VBAT.

If RESET_N is unused, it is recommended to reserve a test point.
9. If pins 16–18, 20–23, 25, 39 and 67 of the module are required, the 22 pF or 33 pF filter capacitors should be reserved and placed near the pins, and the return path for current of capacitors to the main ground should be as short as possible. The capacitance should be selected according to the actual debugging situation.
10. The module supports single USIM card interface by default. If dual USIM card function is required, the analog switch must be added for your design and the module does not support USIM card hot-plug detect function in such case.

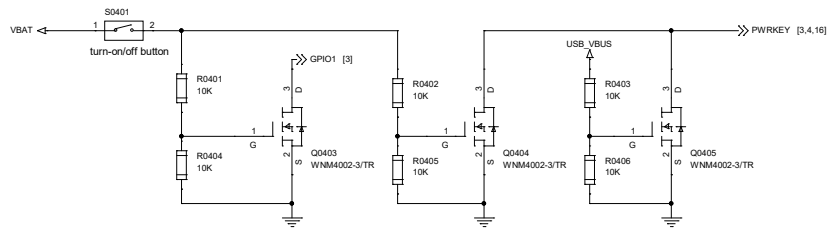


ADC



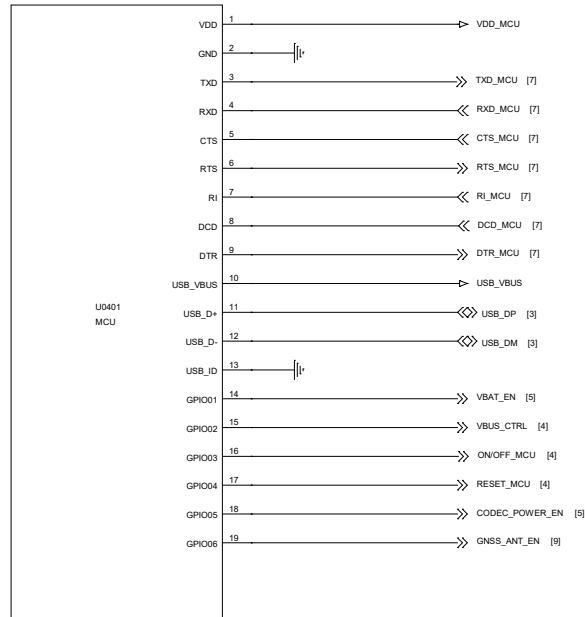
MCU Interfaces

USB Insertion Enables Automatic Boot



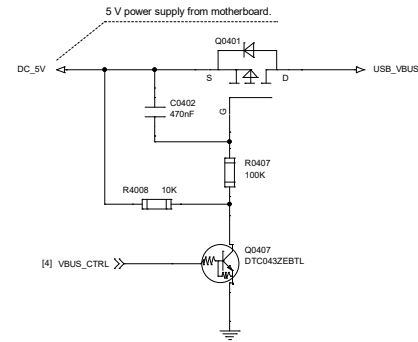
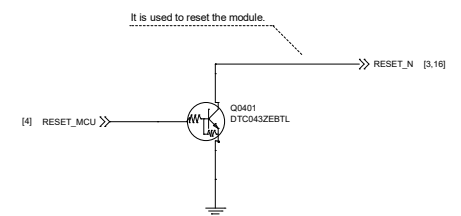
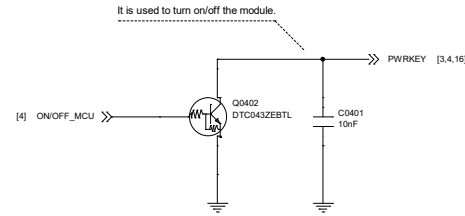
NOTE:

1. When USB is inserted, the module cannot be shut down normally, and will boot automatically after the shut down.
2. When USB is inserted, the level states of GPIO1 and PWRKEY pins are used to determine whether the module is turned on by the turn-on/off button or USB insertion. GPIO1 utilizes the GPIO resource with a default pull-up (PU) state.



NOTE:

1. If the power domain of your MCU (U0401) is also 1.8 V, the level-shifting circuit is not necessary as it matches the 1.8 V power domain of the module's GPIO interfaces.
2. The USB interface of the module can only serve as a slave device and support full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function. For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.



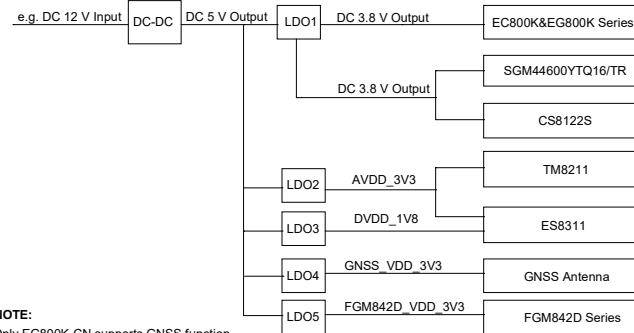
Quectel Wireless Solutions

PROJECT		VER
EC800K&EG800K Series QuecOpen		1.2
DRAWN BY	CHECKED BY	SIZE
Ruben WANG/Kevin SU	Tik HUANG/Stefan FAN	A2
DATE	2025-02-26	SHEET 4 OF 17

Power Supply Design

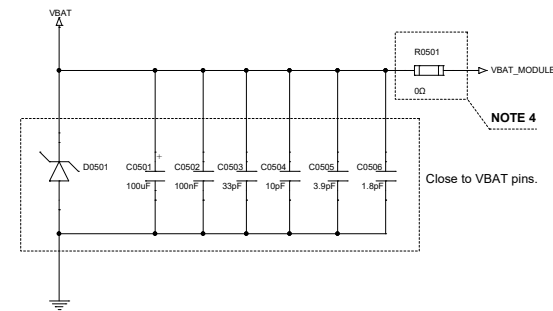
DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, analog switch, audio PA, Codec, GNSS antenna and FGM842D series module.



NOTE:
Only EG800K-CN supports GNSS function.

VBAT Design

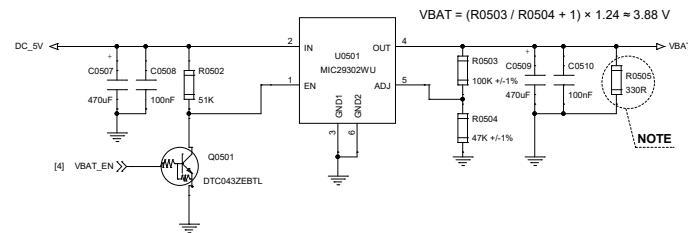


NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 1.5 A.
2. The width of VBAT trace should be at least 2 mm.
3. The recommended operating voltage range for VBAT is 3.4 V to 4.3 V, with a typical value of 3.8 V.
4. It is recommended to reserve a 0 Ω resistor (minimum package size: R-0603) near the VBAT pins for future debugging purposes.

LDO Application

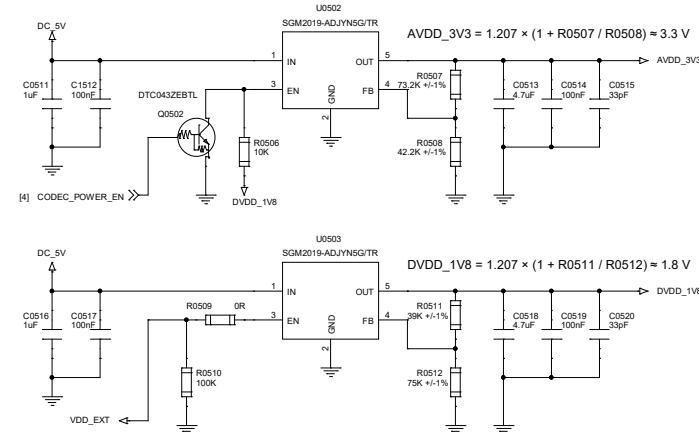
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current should exceed 10 mA.

Power Supply for Codec



NOTE:

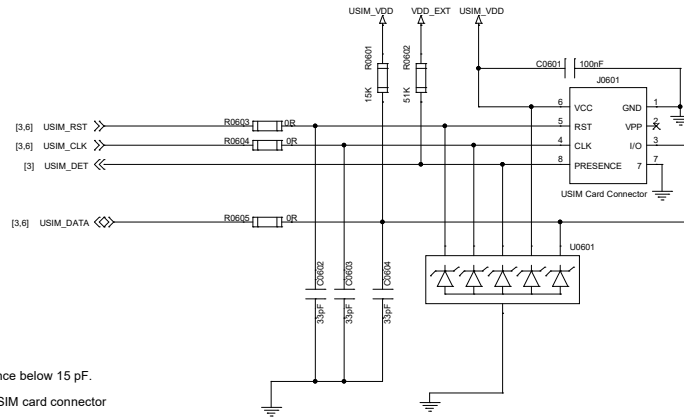
1. VDD_EXT and CODEC_POWER_EN are used to turn on/off DVDD_1V8 and AVDD_3V3 respectively.
2. To ensure proper functioning of the audio codec, adhere to the following power-up/down sequences:
Power-up sequence: power on DVDD_1V8 first, followed by AVDD_3V3.
Power-down sequence: power off AVDD_3V3 first, followed by DVDD_1V8.

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USIM Interface Design

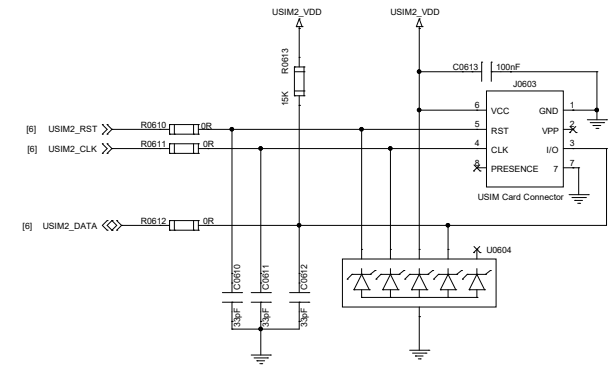
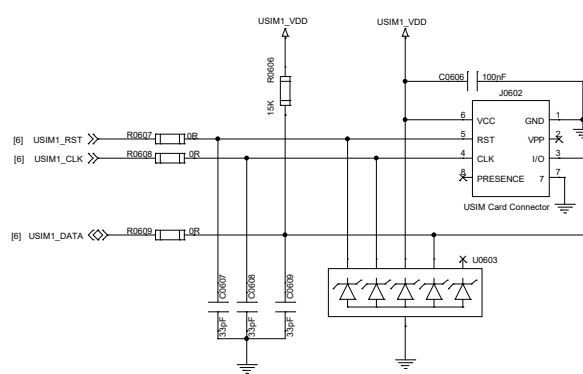
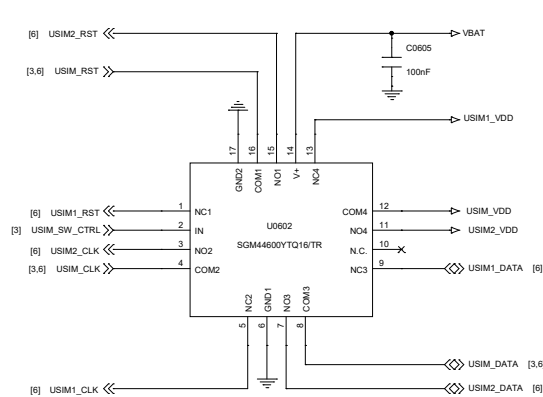
Single USIM Interface Design



NOTE:

1. It is recommended to use U0601 for effective ESD protection with a parasitic capacitance below 15 pF.
2. For USIM_DATA, it is recommended to add a 15 kΩ pull-up resistor R0601 near the USIM card connector to improve the anti-jamming capability of the USIM card.
3. R0603–R0605 are used for debugging, and C0602–C0604 used for filtering out RF interference should be placed close to the USIM card connector.
4. The capacitance of C0601 should be less than 1 μF and it should be placed close to the USIM card connector.

Dual USIM Interface Design (SGM44600YTQ16/TR)



NOTE:

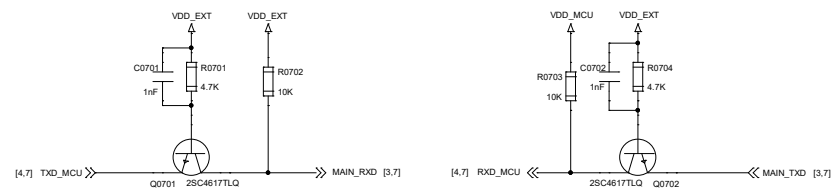
1. It is recommended to use U0603 and U0604 for effective ESD protection with a parasitic capacitance below 15 pF.
2. For USIM1_DATA and USIM2_DATA, it is recommended to add 15 kΩ pull-up resistors R0606 and R0613 respectively near the USIM card connector to improve the anti-jamming capability of the USIM card.
3. R0607–R0612 are used for debugging, and C0607–C0612 used for filtering out RF interference should be placed close to the USIM card connector.
4. The capacitance of C0606 and C0613 should be less than 1 μF and they should be placed close to the USIM card connector.
5. If dual USIM card function is required, an analog switch must be added for your design, and the module does not support USIM card hot-plug detect function in such case.

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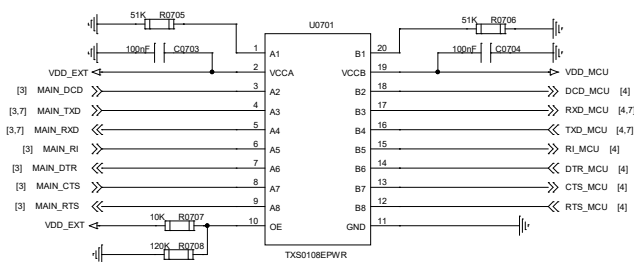
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UART Interface Design

UART Level-shifting Circuit - Transistor Solution

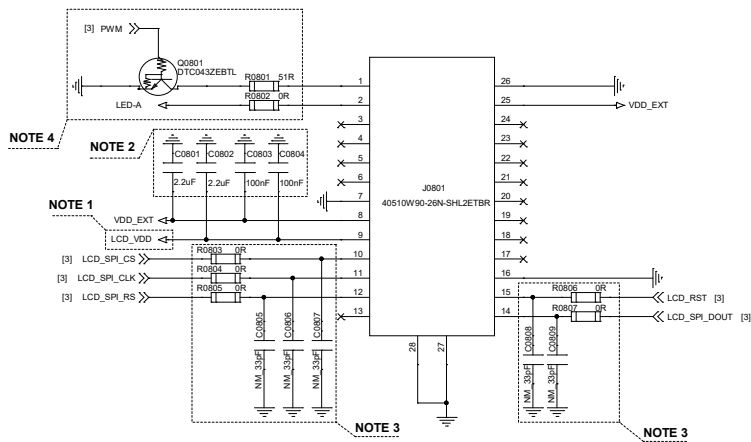


UART Level-shifting Circuit - IC Solution



- NOTE:**
- There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
 - The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
 - The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0701 and C0702 of 1 nF can improve the signal quality.
 - MAIN_RTS and MAIN_DTR's level-shifting circuits are similar to that of the MAIN_RXD.
MAIN_CTS, MAIN_RI and MAIN_DCD's level-shifting circuits are similar to that of the MAIN_TXD.
 - Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART function.
 - To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

LCM Interface Design

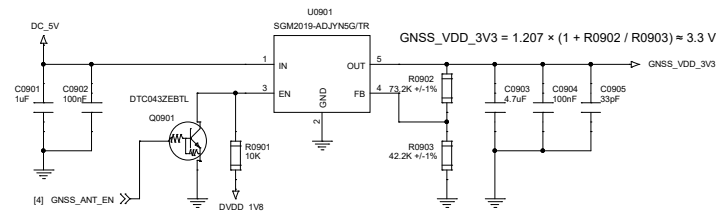


NOTE:

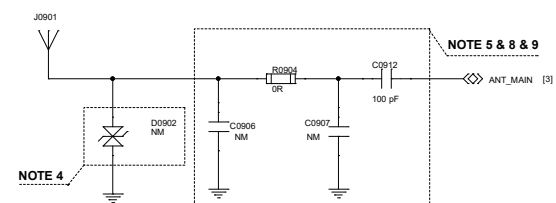
- It is recommended to design LCM power supply by yourself.
- To avoid abnormal LCD display caused by power fluctuation, it is recommended to mount filter capacitors.
- Reserve 33 pF capacitors for the signal pins for debugging.
- The LED-A backlight power supply should be designed by yourself. Select an appropriate resistor (R0801) based on the rated current of the digital transistor and the LED-A voltage value.

Antenna Interface Design

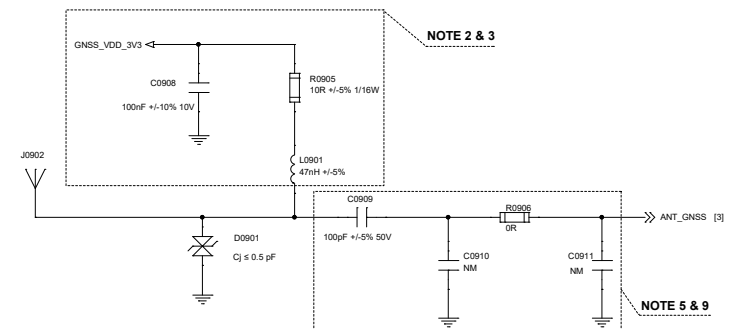
GNSS Active Antenna Power Supply



LTE/Wi-Fi Scan Antenna Design



GNSS Antenna Design



NOTE:

1. Only EG800K-CN supports GNSS function.
2. For active antennas, select an external LDO according to the active antenna types. For passive antennas, the VDD circuit is not necessary.
3. L0901, R0905, C0908 are recommended to be placed close to the RF traces during layout.
4. The junction capacitance of the ESD protection component on the antenna interface is recommended to be less than 0.05 pF.
5. Reserve a dual L-type circuit at antenna interface.
6. The single-ended impedance of the RF antenna is 50 Ω , and length should be minimized.
7. The external active antenna power supply voltage range is 2.8 V to 4.3 V, with a typical value of 3.3 V.

The power supply voltage can be designed according to the power supply requirements of the selected active antenna.

8. Wi-Fi Scan function is optional for EC800K-CN and EG800K-EU/LA, and the function is supported by EG800K-CN.

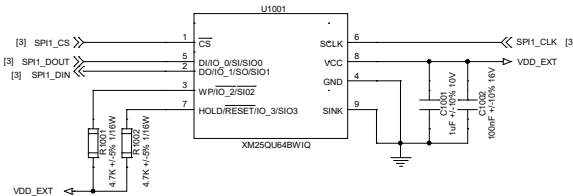
Wi-Fi Scan function shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.

9. Notes on C0909 and C0912:

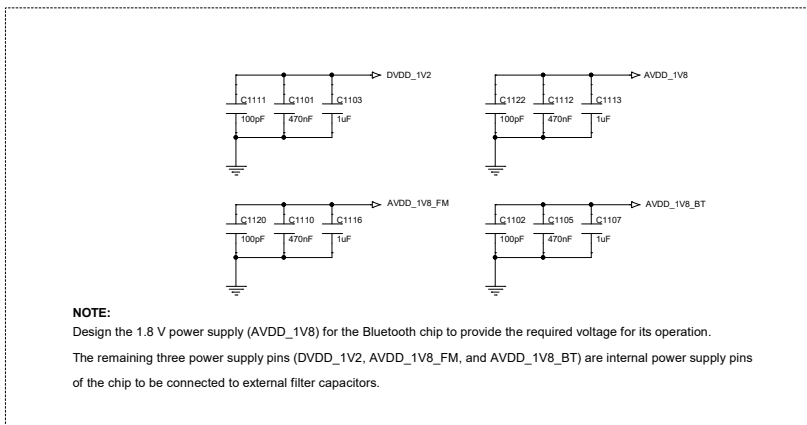
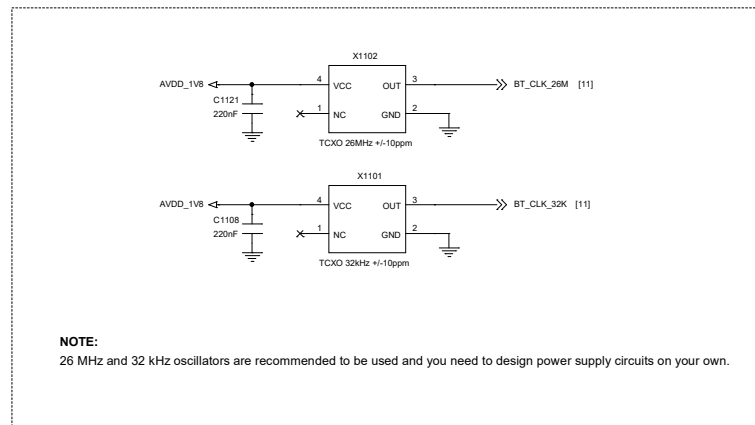
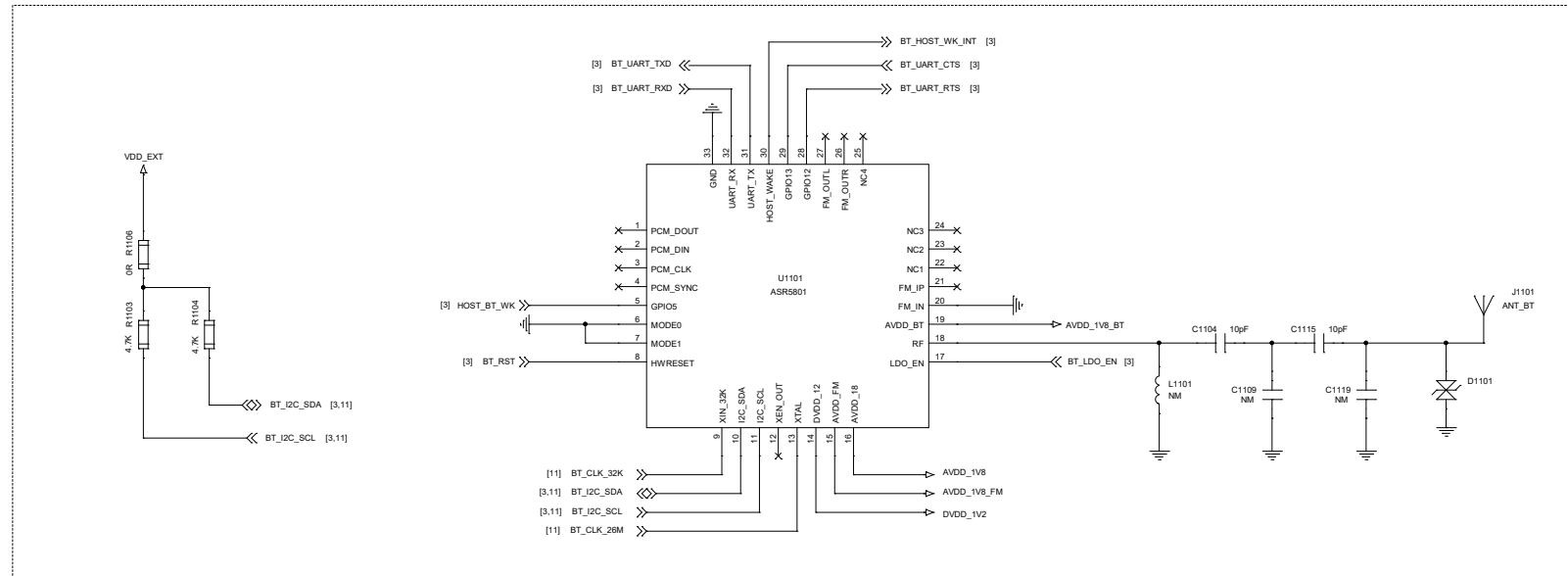
- 1) If there is DC power at the antenna ports, place capacitors on C0909 and C0912 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
- 2) If there is no DC power in the peripheral design:
 - ⊙ Do not reserve C0811 and C0814.
 - ⊙ If C0909 and C0912 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors.

You can also match the components according to the debugging results.

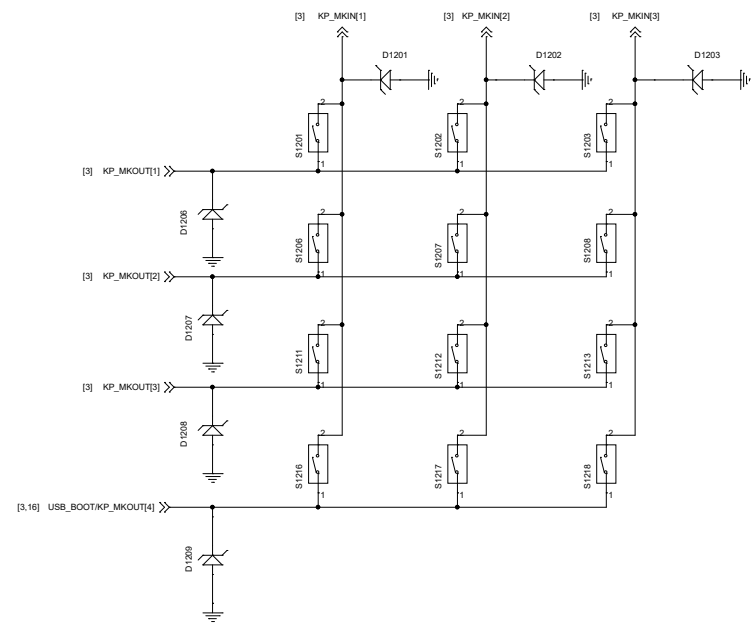
SPI Design



Bluetooth Interface Design

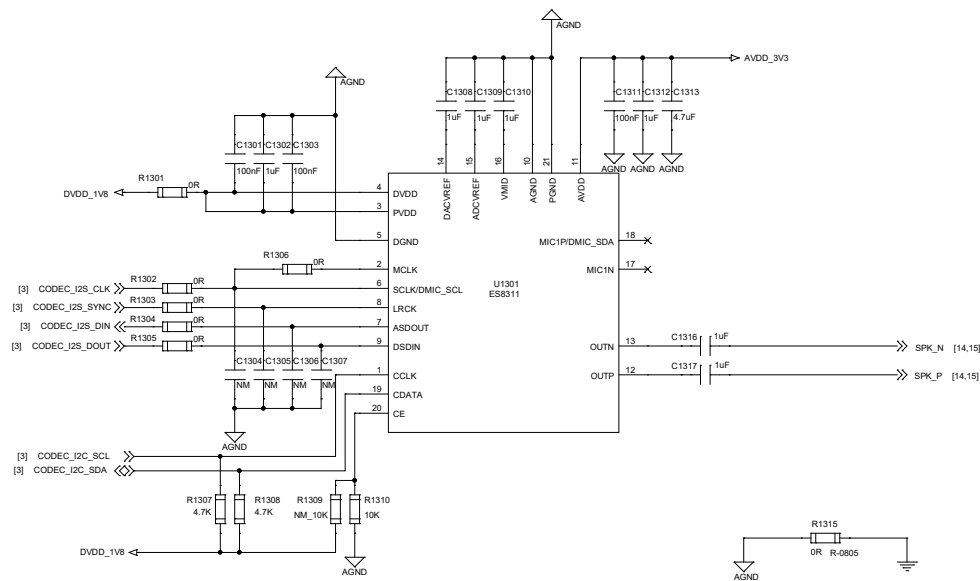


Matrix Keypad Interface Design



Audio Codec Design (ES8311)

ES8311 (Codec)



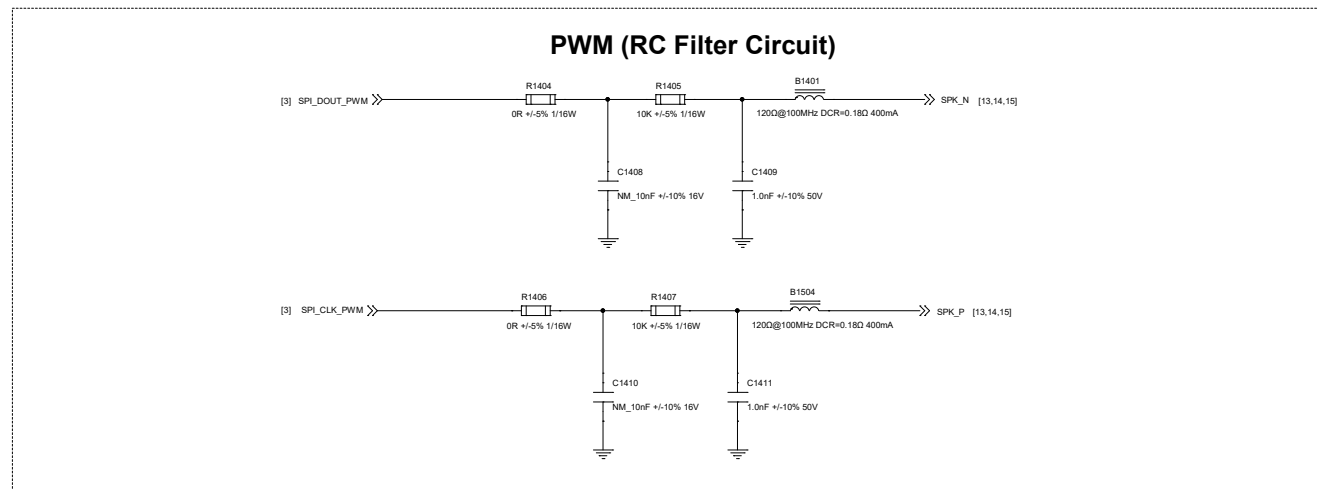
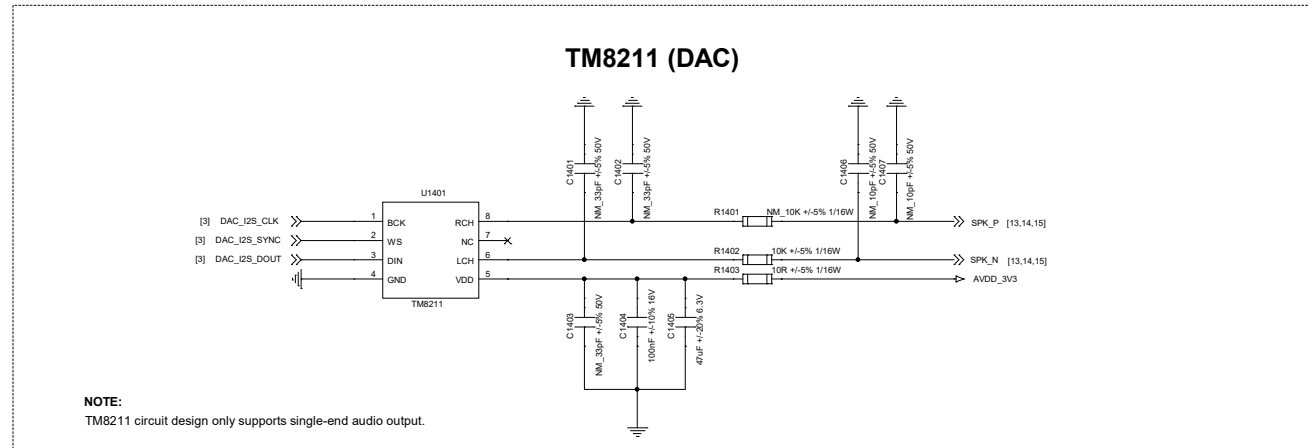
NOTE:

1. When connected to the ES8311, the audio only supports downlink output, and does not support uplink input.
2. Differentiate between analog ground and digital ground. Analog ground should have a direct via to digital GND through a 0 Ω resistor (R-0805).

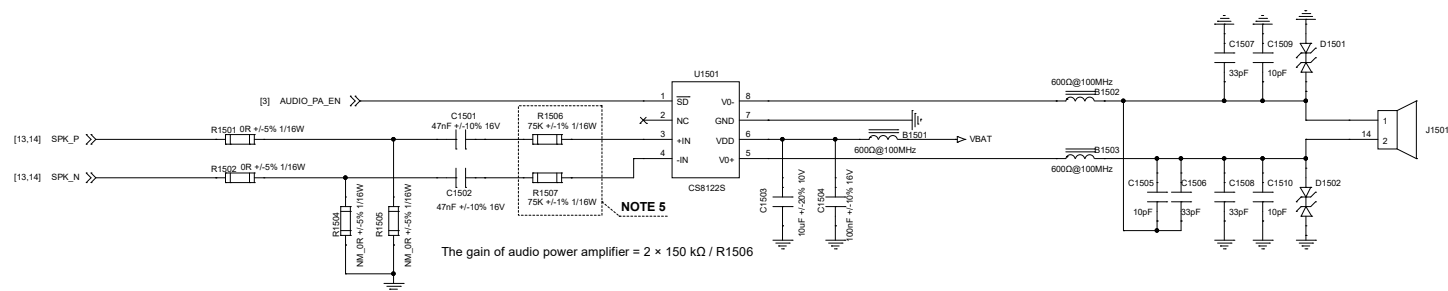
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		SHEET	13 OF 17

Audio Interface Design



Analog Audio Design (Audio Power Amplifier)



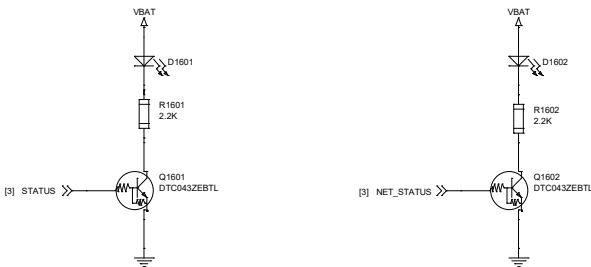
	ES8311	TM8211	PWM
R1501	OR	NM	OR
R1502	OR	OR	OR
R1504	NM	NM	NM
R1505	NM	OR	NM

NOTE:

- SPK_P and SPK_N channels are differential output channels intended for connecting to an external audio power amplifier.
To eliminate Pop noise, it is recommended to utilize MAIN_DCD of the module as the control signal for the audio power amplifier's enable pin.
For more information about AUDIO_PA_EN, please contact Quectel Technical Support.
- The type of power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to your actual needs.
- When designing the layout, ensure that filter capacitors and ESD protection components are placed close to the loudspeaker to filter out interference and provide adequate protection.
- The selection of ESD protection components should consider the output voltage range of the audio power amplifier.
Ensure that the output voltage of the amplifier remains within the maximum reverse working voltage range of the selected ESD protection components under normal operating conditions.
This precaution helps prevent damage to the ESD protection components.
- R1506 and R1507 resistors are used to adjust the audio PA gain which is recommended not exceeding 10 times.

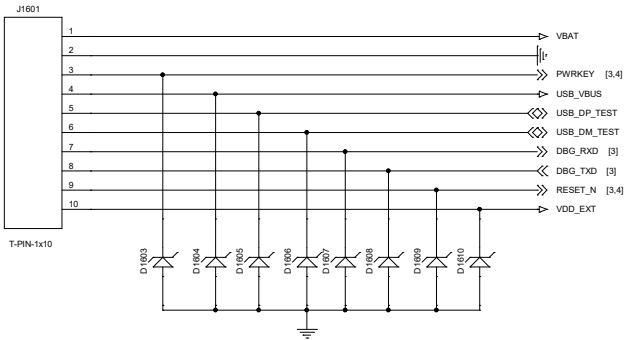
Other Designs

Indicators



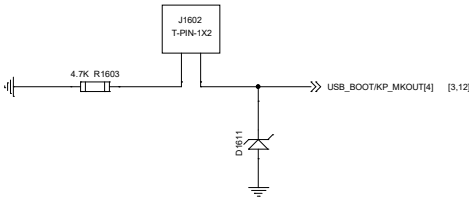
- NOTE:**
- For more details about STATUS and NET_STATUS, see the hardware design document of the module.
 - To minimize the module's power consumption during the sleep mode of your device, replace the power supply (VBAT) of the STATUS and NET_STATUS indicators with externally controllable sources and turn off the indicators when the module is in sleep mode.

Reserved Test Points



- NOTE:**
- Test points for both USB and debug UART interfaces are reserved for capturing logs.
 - Test points for USB interface can also be reserved for firmware upgrade.
 - The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
 - The debug UART interface supports a 1.8 V power domain.
- If your application operates at 3.3 V, use a voltage-level translator.

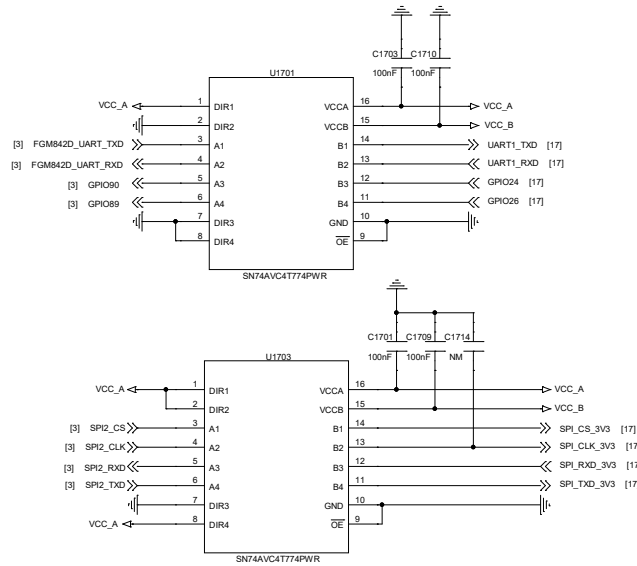
USB_BOOT Interface



- NOTE:**
- Make sure to reserve the USB_BOOT interface design and it is recommended to reserve a test point for USB_BOOT/KP_MKOUT[4].
 - Before turning on the module, pull USB_BOOT/KP_MKOUT[4] down to GND to activate the forced download mode.
This mode enables firmware upgrades via the USB interface.
 - The 6.0 and above version of QFlash tool must be used for firmware upgrades.

Wi-Fi Module Design

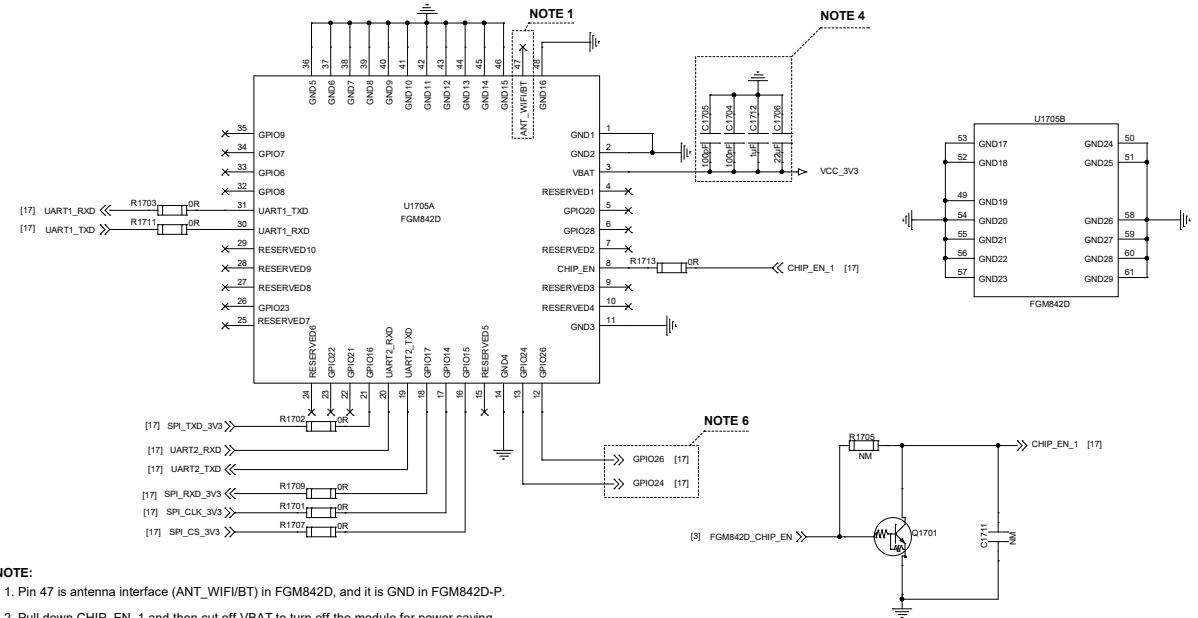
Level-shifting Circuit



NOTE:

1. A voltage-level translator SN74AVC4T774PWR provided by Texas Instruments is recommended.
2. The module's SPI supports master mode with a maximum clock frequency of 26 MHz.

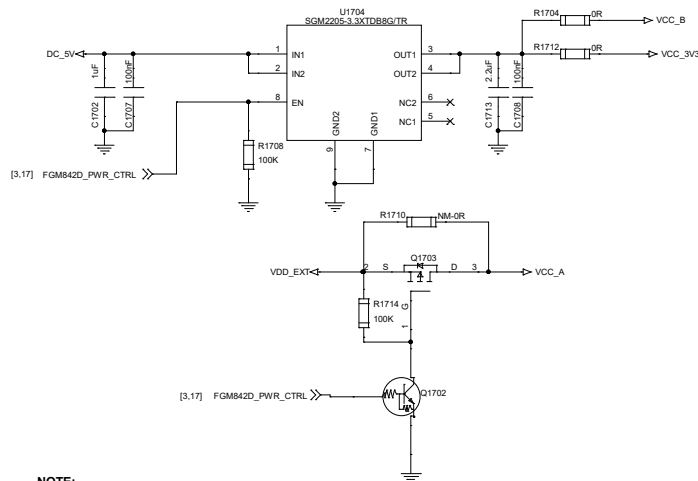
FGM842D Series Design



NOTE:

1. Pin 47 is antenna interface (ANT_WIFI/BT) in FGM842D, and it is GND in FGM842D-P.
 2. Pull down CHIP_EN_1 and then cut off VBAT to turn off the module for power saving.
 3. The firmware for the module will be downloaded when only CHIP_EN_1 is pulled down.
 4. To ensure better power supply performance, it is recommended to place a 22 μ F decoupling capacitor and three filter capacitors (1 μ F, 100 nF and 100 pF) near the module VBAT input.
 5. FGM842D-P provides a PCB antenna only, so it is not necessary to debug the antenna. Please pay attention to the keepout area of PCB antenna.
- For more details, see the hardware design document of the module.
6. GPIO24 and GPIO26 are used for SPI data flow control.

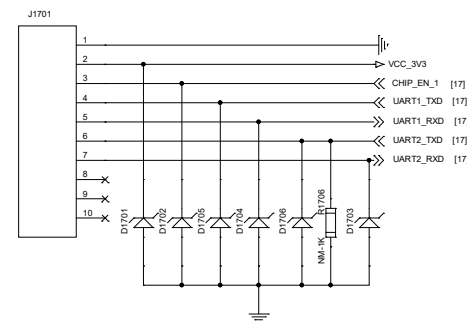
Power Supply Design



NOTE:

The VCC_3V3 trace is recommended to be wider than 0.6 mm. In principle, the longer the VCC_3V3 trace is, the wider it should be. The power supply must be provided with sufficient current of at least 0.6 A.

Reserved Test Points



NOTE:

1. Test points must be reserved.
2. When the FGM842D series module enters ATE (Automatic Test Execution) mode, UART2_TXD needs to be pulled down by a 1 kΩ pull-down resistor.