EC800K&EG800K Series
QuecOpen&QuecPython Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-08-05	Kelly WANG/ Stefan FAN/ Jerry LIN/ Felix YE	Creation of the document
1.0	2024-09-02	Reuben WANG/ Kevin SU/ Jerry LIN/ Felix YE	First official release

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Table Index

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1 Introduction

This document is only applicable to EC800K-CN and EG800K series (consisting of EG800K-CN, EG800K-EU and EG800K-LA) industrial-grade module in QuecOpen® solution.

The document mainly introduces the EC800K-CN and EG800K series modules and their hardware interfaces and air interfaces connected to your applications in QuecOpen® and QuecPython® solutions.

The document can help you quickly understand the hardware interface characteristics, RF characteristics, electrical characteristics, mechanical specifications and other relevant information of the module.

1.1. QuecOpen® Solution Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle;
- Simplify circuit and hardware structure design to reduce engineering costs;
- Miniaturize products;
- Reduce product power consumption;
- Apply OTA technology;
- Enhance product competitiveness and price-performance ratio.

1.2. QuecPython® Solution Introduction

QuecPython® is a Python runtime environment transplanted from MicroPython® open-source library. It is a new IoT development solution based on Quectel's module that uses MircroPython® to invoke the module's software functions and external hardware interfaces to help users perform the secondary development of embedded applications. Its main advantages are as follows:

- Efficient and convenient Python development: provide abundant API to ensure the stability and functions of the interfaces to the greatest extent.
- Compatible with MicroPython®, easy to update and iterate.
- High data security for its architecture.
- Strong portability for its design architecture can be quickly transplanted and adapted to other

application platforms.

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging, which can meet the needs of most M2M applications.

Table 2: Basic Information of EC800K-CN

EC800K-CN	
Packaging type	LCC + LGA
Pin counts	109 pins
Dimensions	(17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 1.27 g

Table 3: Basic Information of EG800K-CN

EG800K-CN	
Packaging type	LGA
Pin counts	109 pins
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 1.37 g

Table 4: Basic Information of EG800K-EU

EG800K-EU	
Packaging type	LGA
Pin counts	109 pins
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (2.4 ±0.2) mm

Weight	Approx. 1.40 g

Table 5: Basic Information of EG800K-LA

EG800K-LA	
Packaging type	LGA
Pin counts	109 pins
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 1.36 g

2.1. Frequency Bands and Functions

Table 6: Frequency Bands and Functions

	EC800K-CN	EG800K-CN	EG800K-EU	EG800K-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B8	B1/B3/B5/B7/B8/ B20/B28	B2/B3/B4/B5/B7 /B8/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	B34/B38/B39/B40/B41	-	-
GNSS	-	GPS/BDS/GLONASS	-	-

NOTE

1. Only EG800K-CN supports GNSS function.
2. LTE-TDD B41 only supports 140 MHz (2535–2675 MHz).

2.2. Key Features

Table 7: Key Features

Category	Description
Supply Voltage	● Supply voltage range: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS (Optional)	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in USIM card and ME, ME by default ● SGS SMS (default)
USB Interface	● Compliant with USB 2.0 specification (only supports slave mode) ● Data transmission rates: up to 480 Mbps ● Used for GNSS NMEA sentence output [1], AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7 and Android 4.x–13.x
USB_BOOT	Supports one forced download interface
USIM Interface	Supports 1.8 V and 3.0 V
UARTs	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for GNSS NMEA sentence output [1] and partial log output ● Baud rate: 115200 bps **Auxiliary UART [2]:** ● Used for communication with peripherals ● Baud rate: 115200 bps
I2C Interfaces	● Supports two I2C interfaces ● Comply with I2C-bus specification
SPI	Supports slave mode* and master mode, with a maximum clock frequency of 26 MHz
LCM Interface	● Supports LCD display module with a maximum resolution of 240 × 320 ● Supports SPI four-wire single-line data transmission ● Supports RGB565 format output

[1] Only EG800K-CN supports GNSS NMEA sentence output.
[2] Only EC800K-CN, EG800K-LA and EG800K-EU support auxiliary UART.

Matrix Keypad Interface	Supports 3 × 4 matrix keypad
ADC Interfaces	Supports two ADC interfaces
Network Indication	NET_STATUS indicates network activity status
Audio Features	● Supports external RC circuit with one audio output ● Supports external Codec chip with one audio output (optional) ● Supports external DAC chip with one audio output (optional)
AT command	● Complies with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Antenna Interfaces	● LTE/Wi-Fi Scan antenna interface [3] (ANT_MAIN) ● GNSS antenna interface [4] (ANT_GNSS) ● 50 Ω characteristic impedance
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-13 Cat 1 bis FDD and TDD ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Max. data rates: – LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) – LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
GNSS Features [4]	● Supports GPS, BDS and GLONASS positioning system ● Supports NMEA 0183 protocol ● Data update rate: 1 Hz ● Supports AGNSS. See ***document [1]*** for more details.
Position Fixing	● Supports Wi-Fi Scan* [3] positioning (shares the main antenna) ● Supports GNSS positioning [5]
Internet Protocol Features [6]	● Compliant with PPP/TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/FILE/MQTT protocols ● Supports PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [7]: -35 °C to +75 °C ● Extended operating temperature [8]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C

[3] The Wi-Fi Scan* function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously.
[4] Only EG800K-CN supports GNSS antenna interface.
[5] Only EG800K-CN supports GNSS positioning.
[6] PPP, FTP, HTTP, HTTPS, FTPS, FILE protocols are optional. PAP and CHAP for PPP connections are optional. For more details, contact Quectel Technical Support.
[7] Within this range, the module's indicators comply with 3GPP specification requirements.
[8] Within this range, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

Firmware Upgrade	Via USB 2.0 interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTE

1. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade. For more details about QPYcom, please visit: https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.
2. The Wi-Fi Scan* function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously.
3. Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART.
4. Only EG800K-CN supports GNSS function.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Flash
- Radio frequency part
- Peripheral interfaces

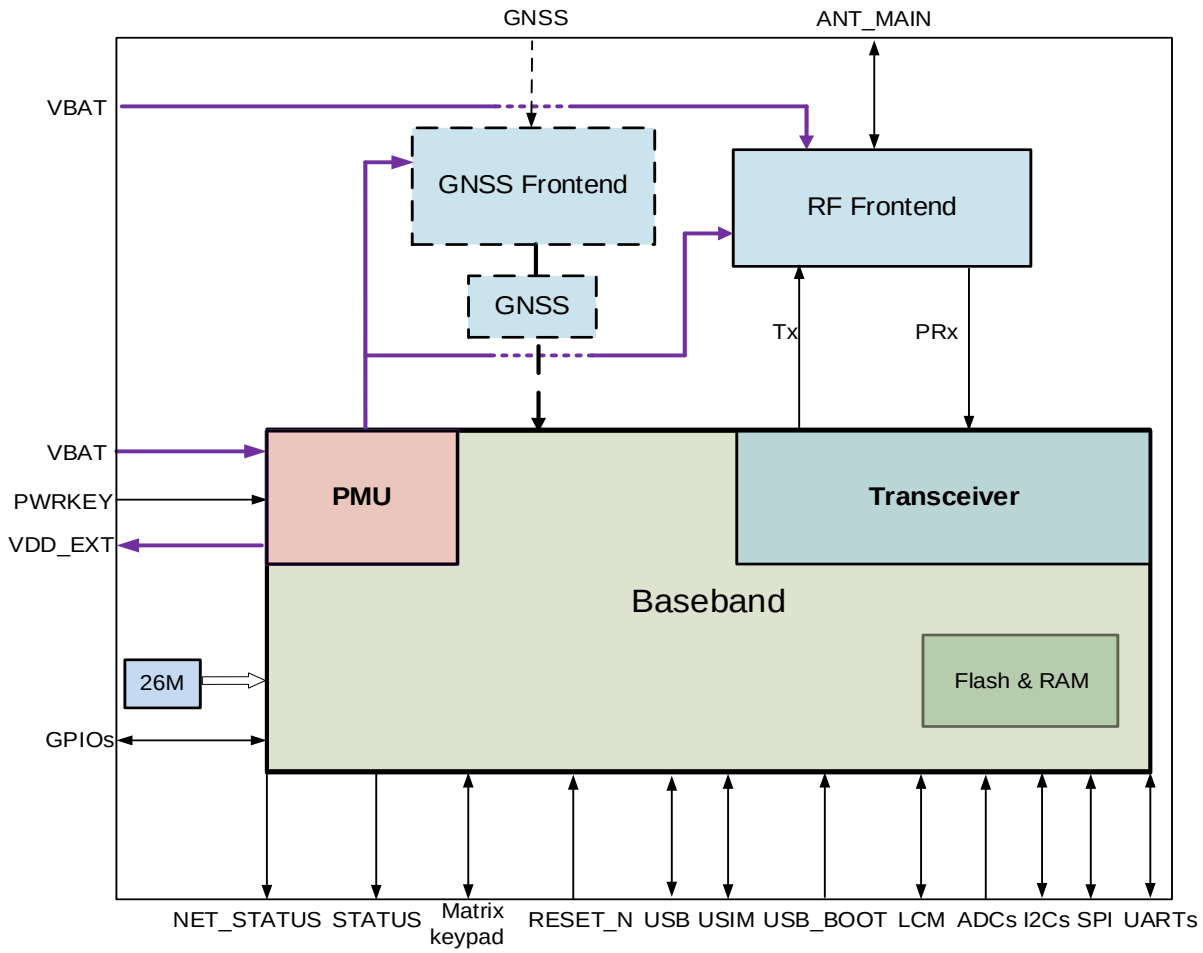


Figure 1: Functional Diagram

NOTE

Only EG800K-CN supports GNSS function.

2.4. Pin Assignment

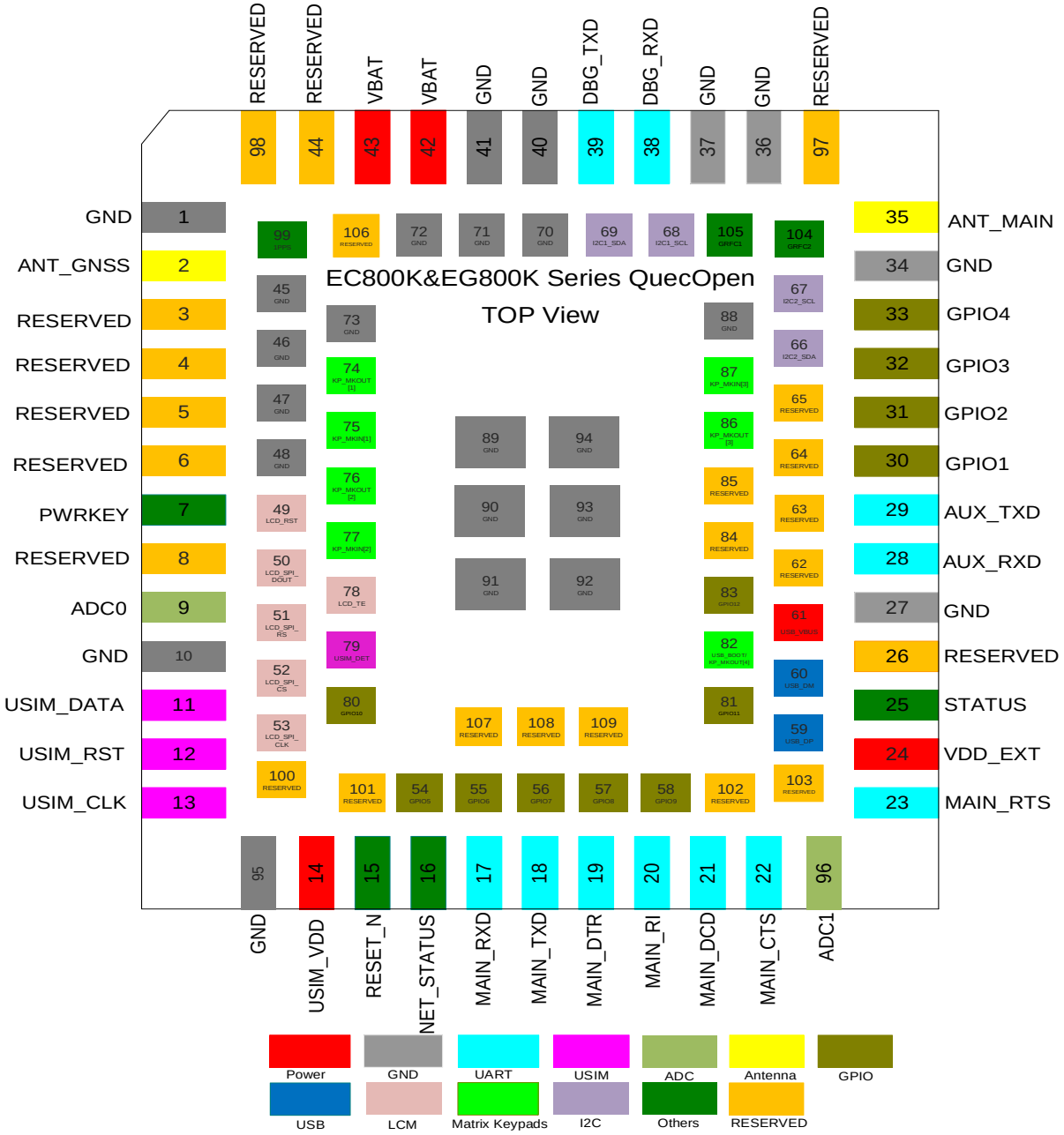


Figure 2: Pin Assignment (Top View)

NOTE

1. Do not pull USB_BOOT/KP_MKOUT[4] down to low level before the module starts up successfully.
2. Keep all RESERVED and unused pins open. Connect all GND pins to the ground.
3. Ensure an uninterrupted reference ground plane below the module, with minimal distance between

the ground plane and the module layer. Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.

4. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade. For more details about QPYcom, please visit: https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.
5. Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART. For EG800K-CN, pins 28, 29, 54–58, 80 are RESERVED.
6. If pins 16–18, 20–23, 25, 39, 67 of the module are required, the 22 pF or 33 pF filter capacitors should be reserved and placed near the pins, and the return path for current of capacitors to the main ground should be as short as possible. The capacitance should be selected according to the actual debugging situation. See ***document [2]*** for details.
7. Only EG800K-CN supports GNSS function. For EC800K-CN, EG800K-EU and EG800K-LA, pins 2 and 99 are RESERVED.

2.5. Pin Definitions

Table 8: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 9: Pin Description

Power Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply should be able to provide with sufficient current of at least 1.5 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95				
Power Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	24	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Turn on/off the module. A test point is recommended to be reserved.
RESET_N	15	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active low. A test point is recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	59	AIO	USB 2.0 differential data (+)		Compliant with USB 2.0 specification. 90 Ω differential impedance is required. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)		
USB_VBUS	61	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DATA	11	DIO	USIM card data	1.8/ 3.0 V	
USIM_RST	12	DO	USIM card reset		
USIM_CLK	13	DO	USIM card clock		
USIM_VDD	14	PO	USIM card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DET	79	DI	USIM card hot-plug detect	1.8 V	If unused, keep it open.
Auxiliary UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V	Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART.
AUX_TXD	29	DO	Auxiliary UART transmit		

					For EG800K-CN, pins 28 and 29 are RESERVED. If unused, keep them open.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	17	DI	Main UART receive	1.8 V	If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit		
MAIN_DTR	19	DI	Main UART data terminal ready		
MAIN_RI	20	DO	Main UART ring indication		
MAIN_DCD	21	DO	Main UART data carrier detect		
MAIN_CTS	22	DO	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SDA	69	OD	I2C1 serial data		An external 1.8 V pull-up resistor is required.
I2C1_SCL	68	OD	I2C1 serial clock		
I2C2_SCL	67	OD	I2C2 serial clock		

I2C2_SDA	66	OD	I2C2 serial data		If unused, keep them open.
GPIO					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	30	DIO	General-purpose input/output	1.8 V	GPIO1–4 can be multiplexed as external audio interfaces. If unused, keep them open.
GPIO2	31	DIO	General-purpose input/output		
GPIO3	32	DIO	General-purpose input/output		
GPIO4	33	DIO	General-purpose input/output		
GPIO5	54	DIO	General-purpose input/output		If unused, keep them open. For EG800K-CN, pins 54–58, 80 are RESERVED, and GPIO function is not supported.
GPIO6	55	DIO	General-purpose input/output		
GPIO7	56	DIO	General-purpose input/output		
GPIO8	57	DIO	General-purpose input/output		
GPIO9	58	DIO	General-purpose input/output		
GPIO10	80	DIO	General-purpose input/output		
GPIO11	81	DIO	General-purpose input/output		If unused, keep them open.
GPIO12	83	DIO	General-purpose input/output		
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	35	AIO	LTE/Wi-Fi Scan* antenna interfaces		50 Ω characteristic impedance.
ANT_GNSS	2	AI	GNSS antenna interface		50 Ω characteristic impedance. Only EG800K-CN supports GNSS function. For EC800K-CN, EG800K-EU and

					EG800K-LA, this pin is RESERVED. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	0–1.2 V	If unused, keep them open.
ADC1	96	AI			
Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	105	DO	Generic RF controller		If unused, keep them open.
GRFC2	104	DO			
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_RST	49	DO	LCD reset	1.8 V	If unused, keep them open.
LCD_SPI_DOUT	50	DO	LCD SPI data output		
LCD_SPI_RS	51	DO	LCD SPI register select		
LCD_SPI_CS	52	DO	LCD SPI chip select		
LCD_SPI_CLK	53	DO	LCD SPI clock		
LCD_TE	78	DI	LCD tearing effect		
Matrix Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
KP_MKOUT[1]	74	DO	Matrix keypad output 1	1.8 V	If unused, keep them open.
KP_MKIN[1]	75	DI	Matrix keypad input 1		
KP_MKOUT[2]	76	DO	Matrix keypad output 2		

KP_MKIN[2]	77	DI	Matrix keypad input 2		
USB_BOOT/ KP_MKOUT[4]	82	DO	Matrix keypad output 4		
KP_MKOUT[3]	86	DO	Matrix keypad output 3		
KP_MKIN[3]	87	DI	Matrix keypad input 3		
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT/ KP_MKOUT[4]	82	DI	Force the module into download mode	1.8 V	Active low. Do not pull it down to a low level before the module starts up successfully. A test point is recommended to be reserved.
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
1PPS	99	DO	GNSS pulse per second output	1.8 V	Do not pull it down when GNSS is powered on. Only EG800K-CN supports GNSS function. For EC800K-CN, EG800K-EU and EG800K-LA, this pin is RESERVED. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	3–6, 8, 26, 44, 62–65, 84, 85, 97, 98, 100–103, 106–109				Keep them open.

NOTE

1. Keep all RESERVED and unused pins open. Connect all GND pins to the ground.
2. Do not pull USB_BOOT/KP_MKOUT[4] down to low level before the module starts up successfully.
3. Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART. For EG800K-CN, pins 28, 29, 54–58, 80 are RESERVED.
4. If pins 16–18, 20–23, 25, 39, 67 of the module are required, the 22 pF or 33 pF filter capacitors should be reserved and placed near the pins, and the return path for current of capacitors to the main ground should be as short as possible. The capacitance should be selected according to the actual debugging situation. See ***document [2]*** for details.
5. Only EG800K-CN supports GNSS function. For EC800K-CN, EG800K-EU and EG800K-LA, pins 2 and 99 are RESERVED.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module. For more details, see ***document [3]***.

3 Operating Characteristics

3.1. Operating Modes

Table 10: Operating Mode Overview

Mode	Description	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. In this mode, the software is active
	Data	Network connection is ongoing. Power consumption is decided by network setting and data transmission rate.
Minimum functionality mode	● API can set the module to the minimum functionality mode without removing the power supply. ● In this mode, both USIM card and RF function are disabled.	
Airplane Mode	● API can set the module to airplane mode. ● In this mode, RF function is disabled.	
Sleep Mode	Power consumption of the module will be reduced to an ultra-low level. The module can still receive paging message, SMS and TCP/UDP data from the network.	
Power Down Mode	PMU shuts down the power supply. In this mode, software is not active. However, the voltage supply for VBAT remains applied.	

The following table shows the related API used for operating modes.

Table 11: Related API of Operating Modes

		QuecOpen	QuecPython
	API	*ql_dev_set_modem_fun()*	*net.setModemFun()*
Minimum functionality mode (both RF function and USIM card are disabled)	Values of *Function/fun*	*QL_DEV_MODEM_MIN_FUN*	0
Full Functionality Mode (default)		*QL_DEV_MODEM_FULL_FUN*	1

Airplane Mode (RF function is disabled)	*QL_DEV_MODEM_DISBLE_TRANSMIT_AND_RECEIVE_RF_CIRCUITS*	4

NOTE

For more details about API of operating modes:

- QuecOpen: See ***document [4]***.
- QuecPython: Please visit: https://python.quectel.com/doc/API_reference/zh/iotlib/net.html.

3.2. Sleep Mode

With DRX technology, power consumption of the module can be reduced to an ultra-low level.

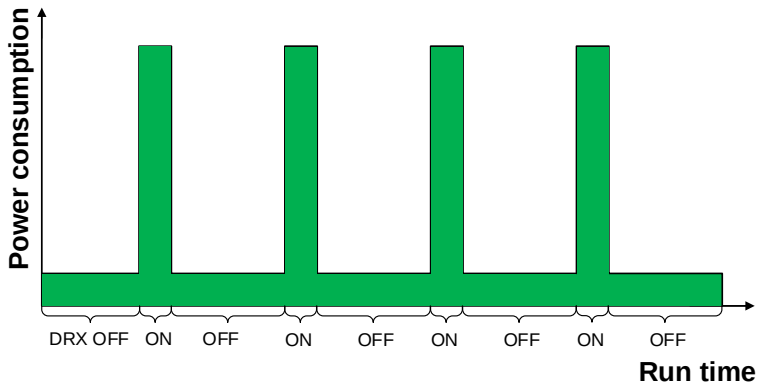


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

Three preconditions must be met to set the module to sleep mode:

- Enable sleep function through API.
- All GPIOs which can be configured as interrupt wake-up function are in non-wake-up state.
- Disconnect USB_VBUS.

The following API can be used to enable sleep mode:

Table 12: Related API of Enabling Sleep Mode

	QuecOpen	QuecPython
API	*ql_autosleep_enable()*	*pm.autosleep()*

The reference figure shows the connection between the module and the host.

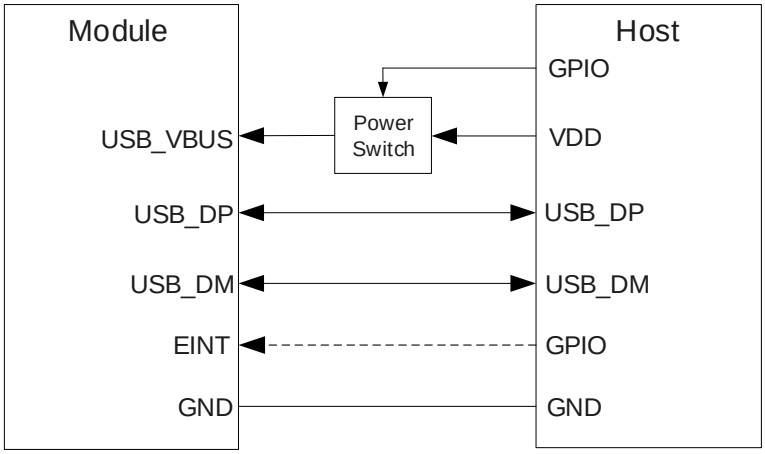


Figure 4: Sleep Mode Application

Resume USB_VBUS power supply or use GPIO interrupts to wake up the module.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the host.
2. For more details about API of enabling sleep mode:
   - QuecOpen: See ***document [5]***.
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/syslib/pm.html.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all APIs related to the RF function will be inaccessible.

The airplane mode can be set through API and set values of *function* or *fun*. For more details, see ***Table 11***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides two VBAT pins for connection with the external power supply:

Table 13: Pin Description of Power Supply Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT	42, 43	PI	Power supply for the module	External power supply should be able to provide with sufficient current of at least 1.5 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95			

3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of at least 1.5 A. If the voltage difference between the input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The figure below is a reference design for a 5 V supply circuit.

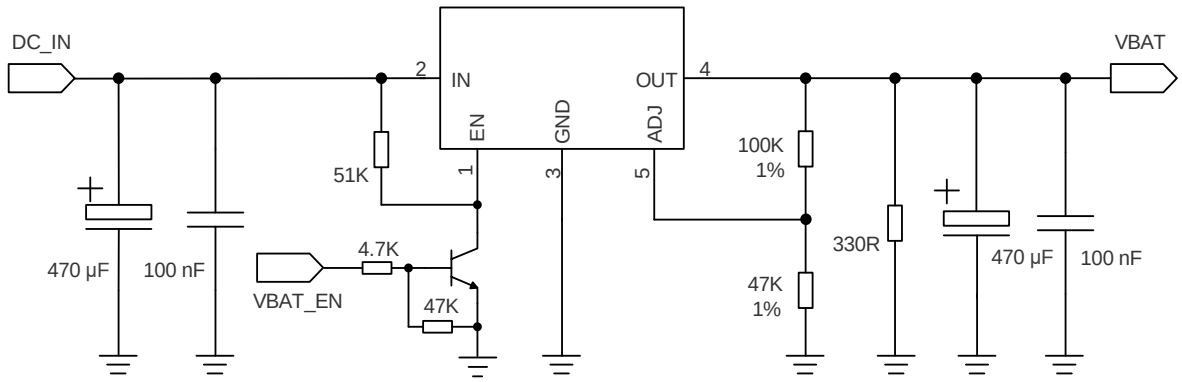


Figure 5: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or API can you cut off the power supply.

3.4.3. Power Supply Voltage Monitoring

You can use the following APIs to monitor and query the VBAT_BB voltage.

Table 14: Related API of Monitoring Power Supply Voltage

	QuecOpen	QuecPython
API	*ql_get_battery_vol()*	*Power.getVbatt()*

NOTE

For more details about API of monitoring power supply voltage:

- QuecOpen: See ***document [6]***.
- QuecPython: Please visit: https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.4.4. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

To decrease the voltage drop, use a filter capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω). Reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR and one 0 Ω resistor (the package should be at least 0603). It is recommended to use five ceramic capacitors (1.8 pF, 3.9 pF, 10 pF, 33 pF and 100 nF) for composing the MLCC array, and place the capacitors and the resistor close to the VBAT pins. When the external power supply is connected to the module, the width of VBAT trace should not be less than 2 mm. As per design rules, the longer the VBAT trace is, the wider it should be.

To ensure the stability of the power supply to the module, add a TVS component with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply. The reference design is as follows:

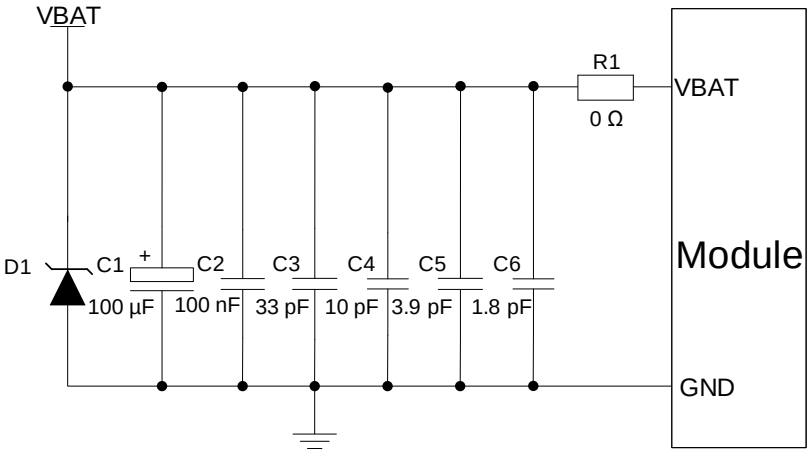


Figure 6: Reference Design of Power Supply

3.5. Turn-on

3.5.1. Turn-on with PWRKEY

Table 15: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 700 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

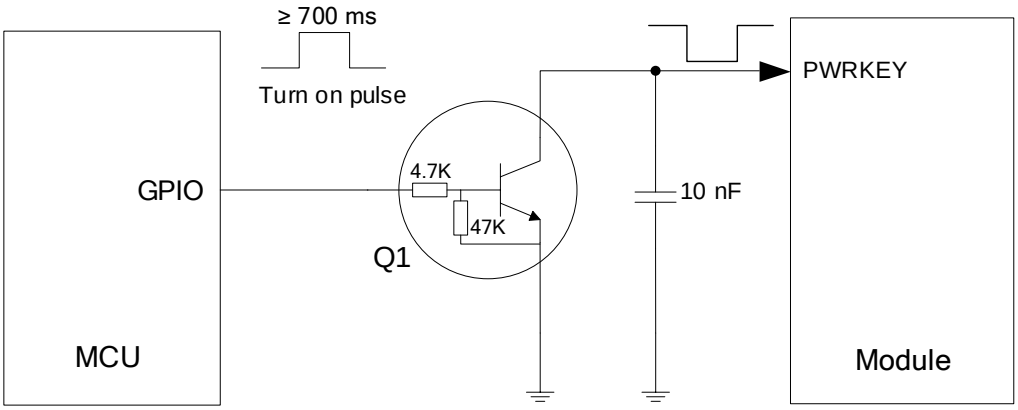


Figure 7: Reference Design of Turn-on with Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS component should be placed near the button for ESD protection.

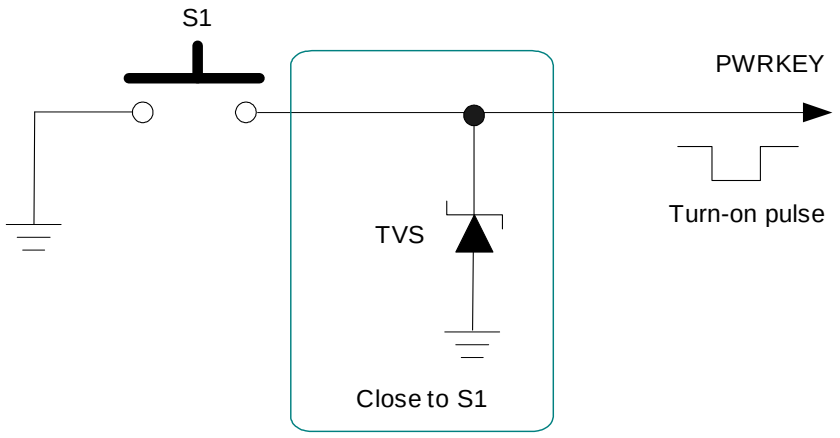


Figure 8: Reference Design of Turn-on with Button

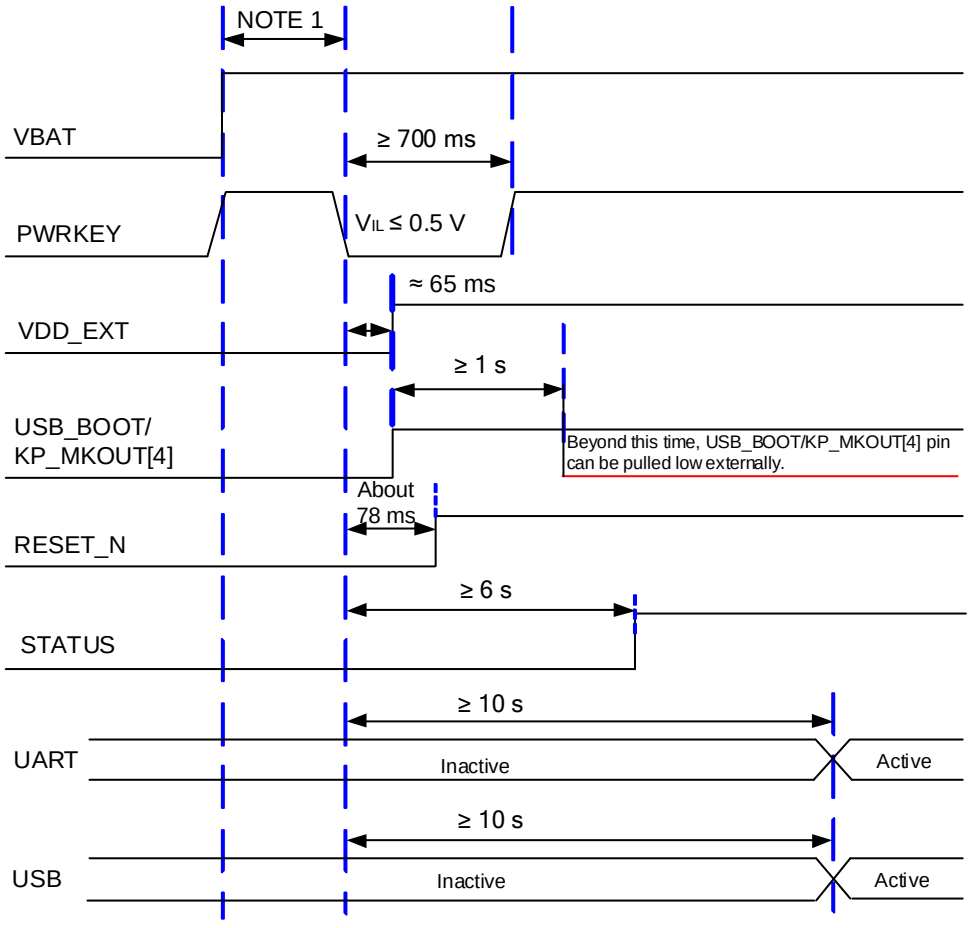


Figure 9: Timing of Turn-on with PWRKEY

NOTE

1. Ensure that VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn-off

3.6.1. Turn-off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it, and the module will execute power-down procedure.

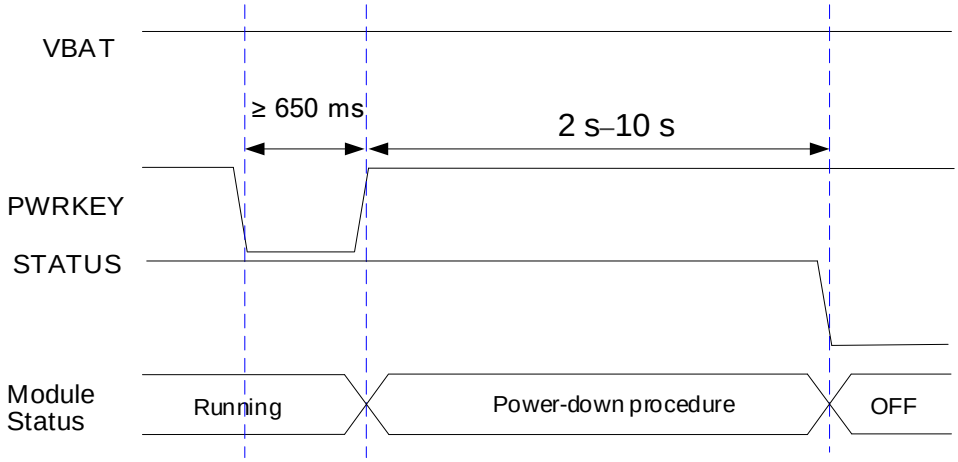


Figure 10: Timing of Turn-off with PWRKEY

3.6.2. Turn-off with API

To turn off the module, you can also execute APIs, which has similar timing and effect as turning off the module through driving PWRKEY low.

Table 16: Related API of Turning off the Module

	QuecOpen	QuecPython
API	*ql_power_down()*	*Power.powerDown()*

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or API can you cut off the power supply.
2. When turning off the module with the API, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.
3. For more details about API of turning off the module:
   - QuecOpen: See ***document [7]***.
   - QuecPython: Please visit: https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.7. Reset

Driving RESET_N low for at least 300 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible a nd surround it with ground.

Table 17: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

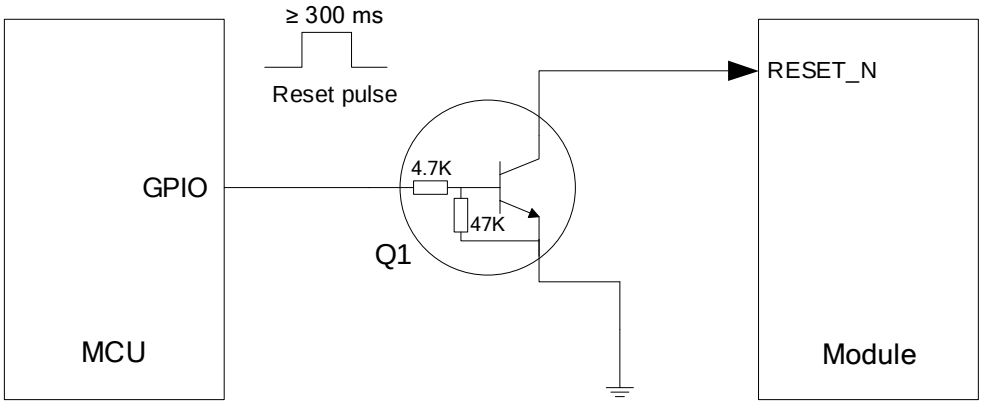


Figure 11: Reference Design of Reset with Driving Circuit

You can also use a button to control RESET_N.

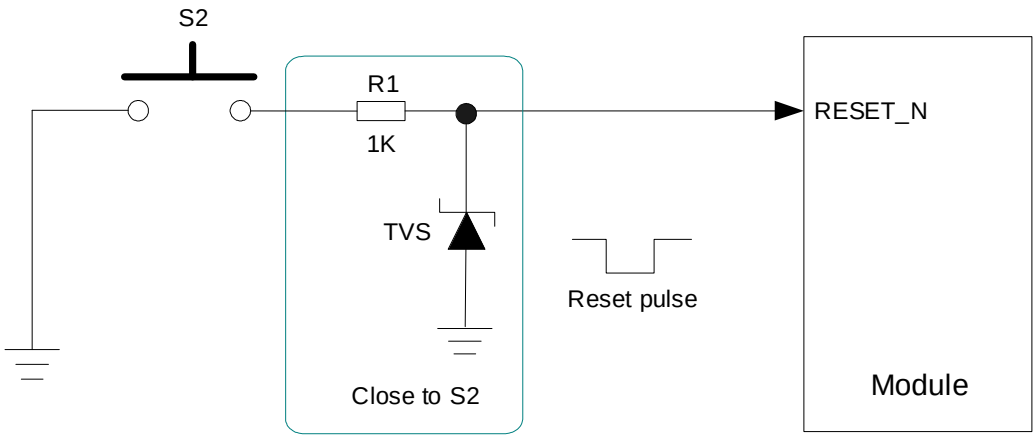


Figure 12: Reference Design of Reset with a Button

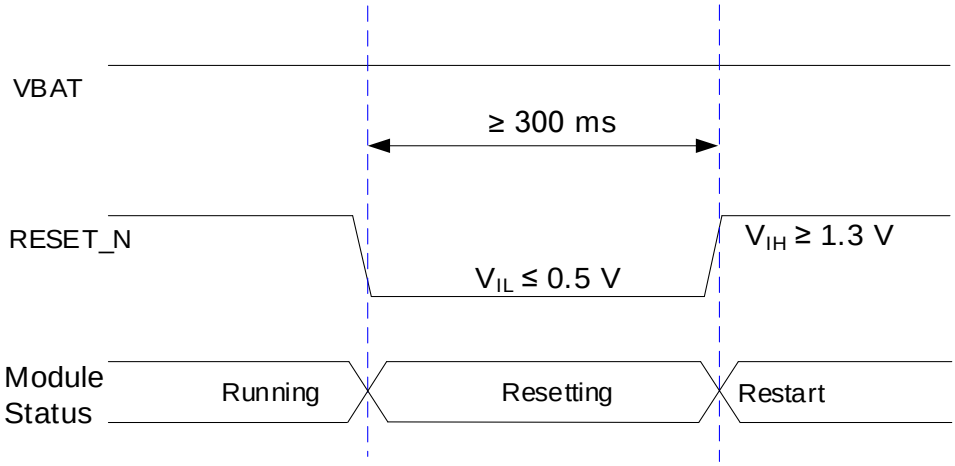


Figure 13: Timing of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the API and PWRKEY.
2. Ensure the capacitance on PWRKEY and RESET_N never exceeds 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which supports slave mode only. It complies with USB 2.0 specification, and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) on USB 2.0. The USB interface can be used for GNSS NMEA sentence output [9], AT command communication, data transmission, software debugging and firmware upgrade.

Table 18: Pin Description of USB interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	59	AIO	USB 2.0 differential data (+)	Compliant with USB 2.0 specification. 90 Ω differential impedance is required. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)	
USB_VBUS	61	AI	USB connection detect	Typical: 5.0 V. A test point must be reserved.

It is recommended to use USB 2.0 interface for firmware upgrade, and test points must be reserved for software debugging.

[9] Only EG800K-CN supports GNSS NMEA sentence output.

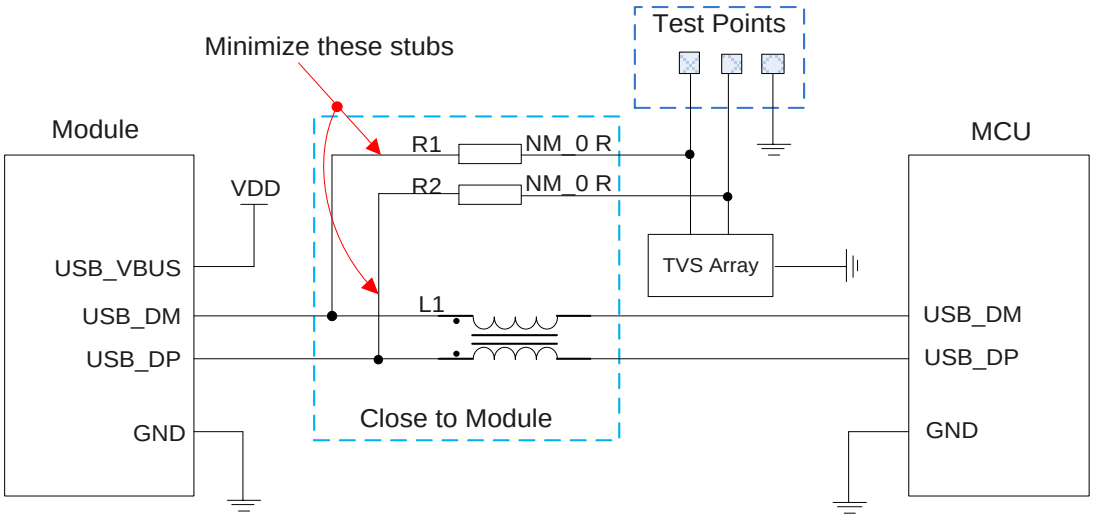


Figure 14: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, the R1 and R2 should be added in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data traces, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, the extra stubs of trace must be as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- The impedance of USB differential trace is 90 Ω. Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock and DC-DC.
- Pay attention to the impact caused by junction capacitance of the ESD protection component on USB data traces. Typically, the junction capacitance should be less than 2 pF and should be placed as close as possible to the USB connector.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT for forced download. Pulling down USB_BOOT/KP_MKOUT[4] to GND before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 19: Pin Description of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT/ KP_MKOUT[4]	82	DI	Force the module into download mode	Active low. Do not pull it down to a low level before the module starts up successfully. A test point is recommended to be reserved.

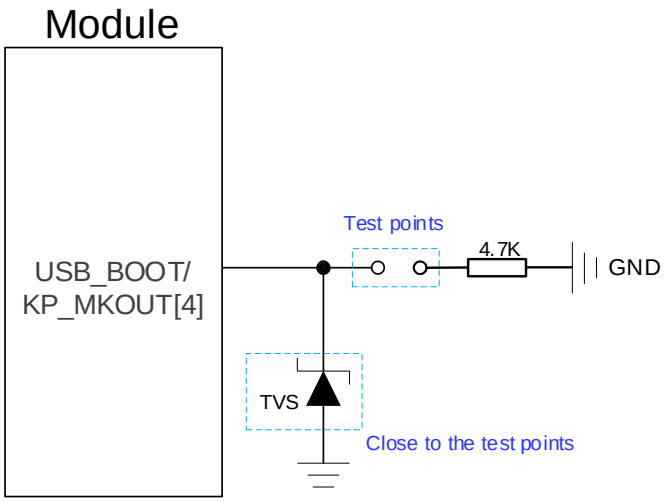


Figure 15: Reference Design of USB_BOOT

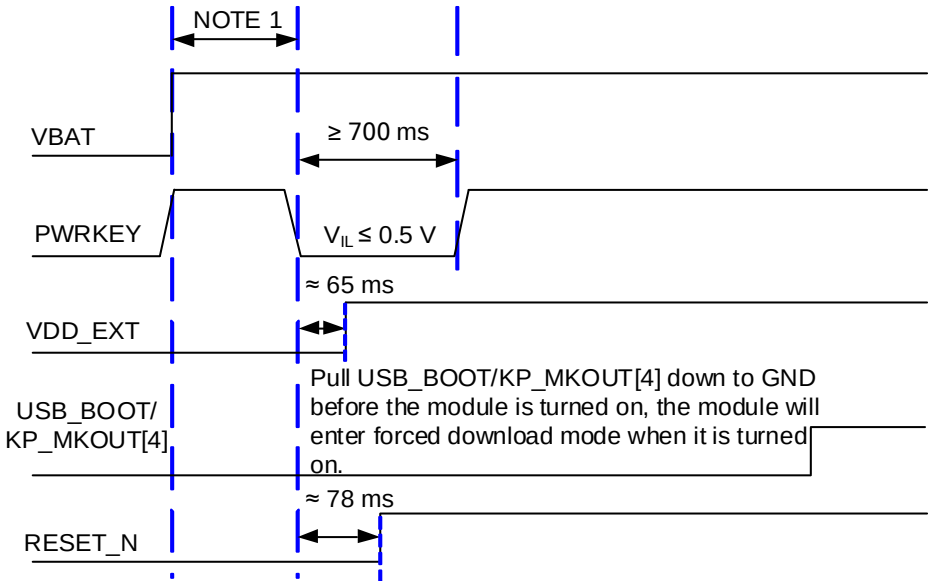


Figure 16: Timing of Entering Forced Download Mode

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. Follow the above timing when using MCU to control module to enter the forced download mode. If you need to manually force the module to enter forced download mode, directly connect the test points shown in ***Figure 15***.
3. If pull USB_BOOT/KP_MKOUT[4] down to GND, the resistor is recommended to be 4.7 kΩ.
4. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade. For more details about QPYcom, please visit: https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

4.3. USIM Interface

The module provides one USIM interface, which meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported.

Table 20: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DATA	11	DIO	USIM card data	
USIM_RST	12	DO	USIM card reset	
USIM_CLK	13	DO	USIM card clock	
USIM_VDD	14	PO	USIM card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DET	79	DI	USIM card hot-plug detect	If unused, keep it open.

The module supports USIM card hot-plug via USIM_DET (level trigger pin), and both high-level and low-level detections are supported.

The reference circuit of the USIM interface with an 8-pin USIM card connector is as follows：

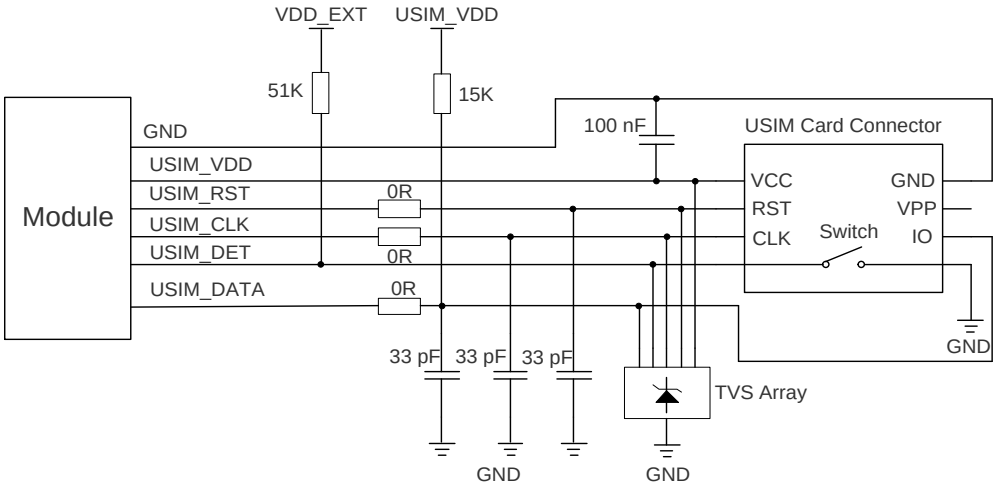


Figure 17: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the USIM card hot-plug detect function is not needed, keep USIM_DET open. The reference circuit of the USIM interface with a 6-pin SIM card connector is as follows.

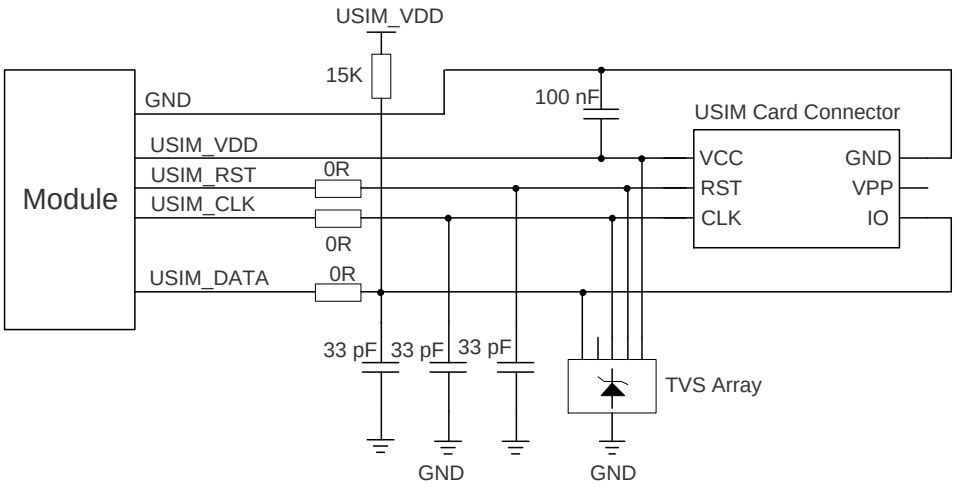


Figure 18: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To ensure performance and reliability, follow the principles below in USIM interface design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signals away from RF and power supply traces.
- Ensure the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and the capacitor should be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should not

exceed 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference. The peripheral components of the USIM card should be placed as close as possible to the USIM card connector.

- For USIM_DATA, it is recommended to add a pull-up resistor near the USIM card connector to improve the anti-jamming capability of the USIM card. When the routing trace of USIM card is too long or there is a relatively close interference source, it is recommended to add a pull-up resistor near the card connector.

NOTE

The module supports single USIM card by default. If dual USIM card function is required, an analog switch should be added for switching. In this case, the module does not support hot-plug detection. See ***document [2]*** for details.

4.4. UARTs

The module provides three UARTs: main UART, debug UART and auxiliary UART.

Table 21: UART Information

UART Type	Supported Baud rate (bps)	Default Baud rate (bps)	Description
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	Used for data transmission and AT command communication; Supports RTS and CTS hardware flow control
Debug UART	115200	115200	Used for GNSS NMEA sentence output [10] and partial log output
Auxiliary UART	115200	115200	Used for communication with peripherals

[10] Only EG800K-CN supports GNSS NMEA sentence output.

Table 22: Pin Description of UARTs

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RXD	17	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit	
MAIN_DTR	19	DI	Main UART data terminal ready	
MAIN_RI	20	DO	Main UART ring indication	
MAIN_DCD	21	DO	Main UART data carrier detect	
MAIN_CTS	22	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V power domain. Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART. For EG800K-CN, pins 28 and 29 are RESERVED. If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit	
DBG_RXD	38	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit	

The module provides 1.8 V UART. You can use a voltage-level translator between the module and MCU's UART if the MCU is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design:

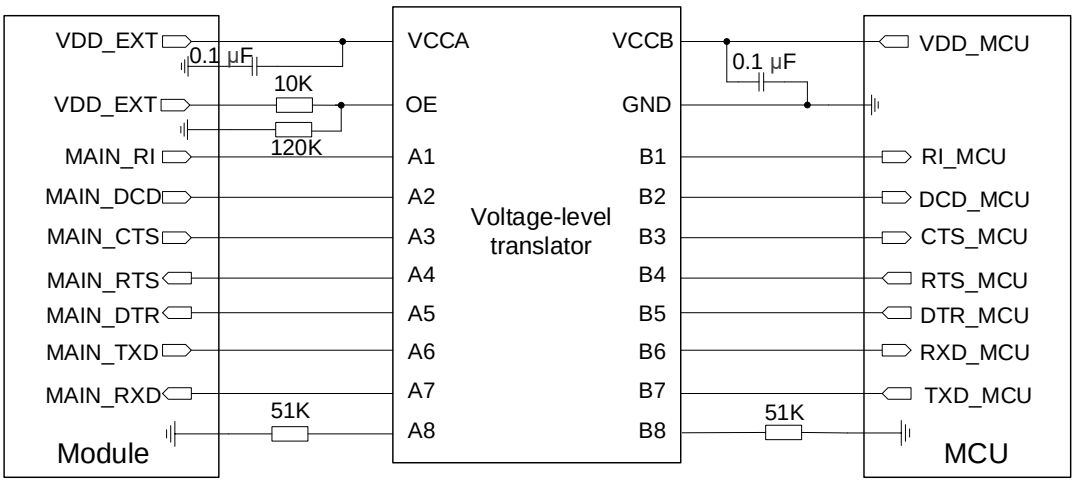


Figure 19: Reference Design of UART with Voltage-level Translator

Another example of level-shifting circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

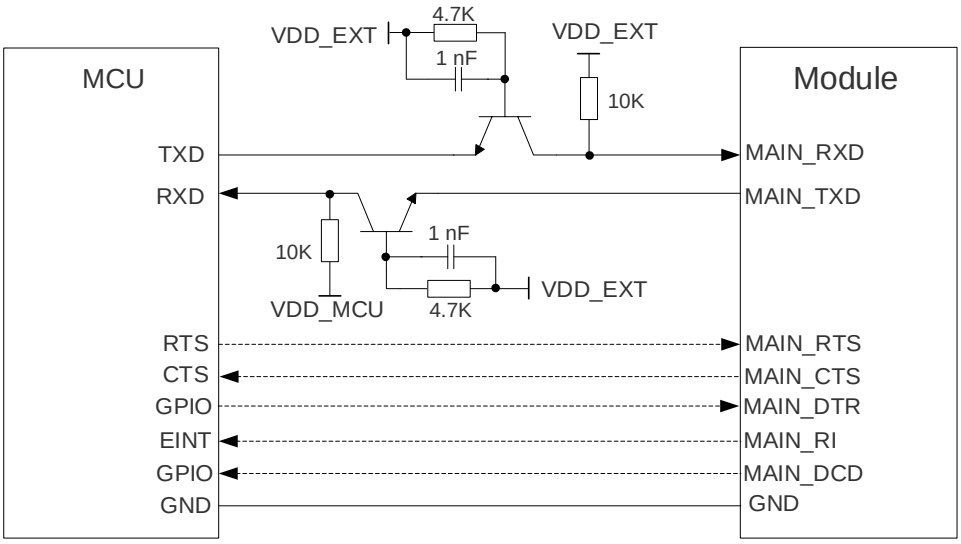


Figure 20: Reference Design of UART with Transistor Level-shifting Circuit

NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. Only EC800K-CN, EG800K-EU and EG800K-LA support auxiliary UART.

4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. I2C Interfaces

The module supports two I2C interfaces.

Table 23: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	69	OD	I2C1 serial data	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C1_SCL	68	OD	I2C1 serial clock	
I2C2_SCL	67	OD	I2C2 serial clock	
I2C2_SDA	66	OD	I2C2 serial data	

4.6. Audio Interface

GPIOs can be multiplexed as SPI to realize audio output function. Audio driver signal can be output through dedicated SPI_DOUT. And audio output function can be realized through external Codec or DAC chip of dedicated SPI. Different external circuit solutions can be selected according to the actual situation.

Table 24: Pin Description of External RC Circuit

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO3	32	SPI0_DOUT	DO	SPI data output	If unused, keep them open.
GPIO1	30	SPI0_CLK	DO	SPI clock	

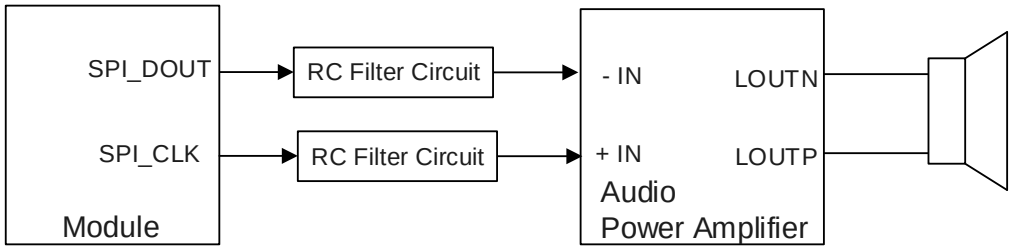


Figure 21: Reference Design of External RC Circuit

Table 25: Pin Description of External Codec Circuit

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO2	31	SPI0_CS	DO	SPI channel can output I2S format, and be used as I2S_SYNC	If unused, keep them open.
GPIO3	32	SPI0_DOUT	DO	SPI channel can output I2S format, and be used as I2S_DOUT	
GPIO4	33	SPI0_DIN	DI	SPI channel can output I2S format, and be used as I2S_DIN	
GPIO1	30	SPI0_CLK	DO	SPI channel can output I2S format, and be used as I2S_CLK	
I2C2_SDA	66	CI2C_SDA	OD	I2C serial data	An external 1.8 V pull-up resistor is needed.
I2C2_SCL	67	CI2C_SCL	OD	I2C serial clock	

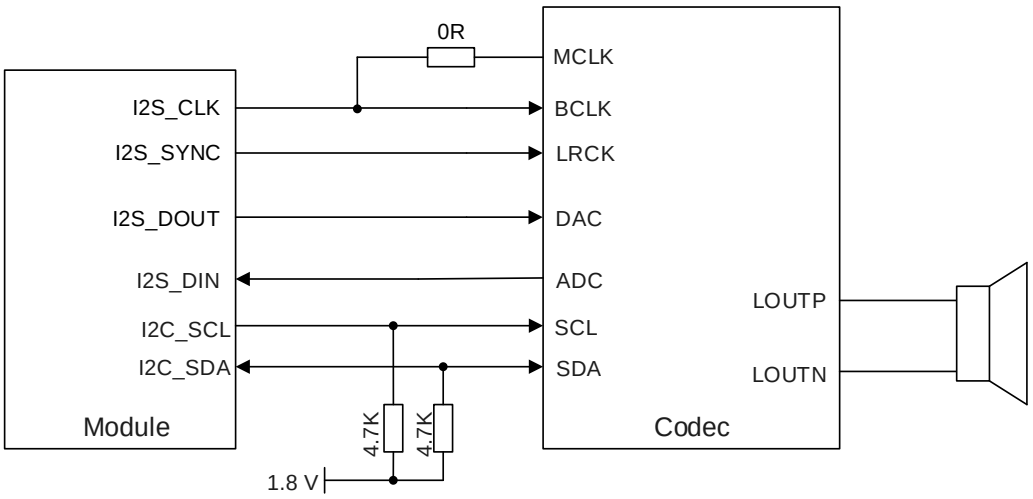


Figure 22: Reference Design of External Codec Circuit

Table 26: Pin Description of External DAC Circuit

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO2	31	SPI0_CS	DO	SPI channel can output I2S format, and be used as I2S_SYNC	If unused, keep them open.
GPIO3	32	SPI0_DOUT	DO	SPI channel can output I2S format, and be used as I2S_DOUT	
GPIO1	30	SPI0_CLK	DO	SPI channel can output I2S format, and be used as I2S_CLK	

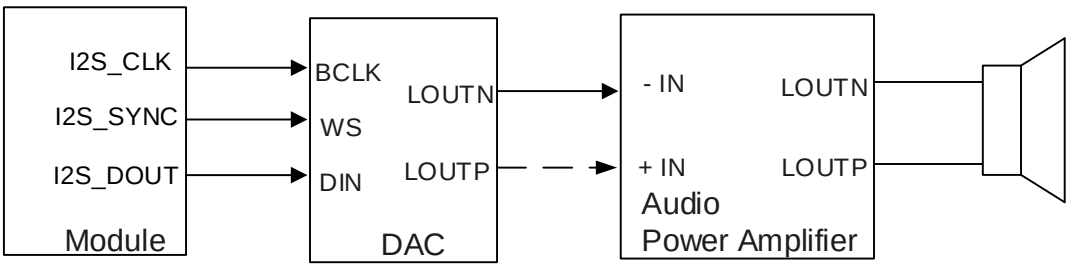


Figure 23: Reference Design of External DAC Circuit

NOTE

1. RC filter circuit design is used for external audio by default. External Codec chip or DAC chip circuit design can be selected to meet higher audio requirements.
2. When using the external Codec circuit, only the down-link output is supported, and the up-link input is not supported.
3. When using the external DAC circuit, the output of the DAC model should be confirmed. For single-ended output, the audio power amplifier should provide single-ended input.
4. It is recommended that the gain of the audio power amplifier does not exceed 10 times.

4.7. SPI

The module provides one SPI, which supports slave mode* and master mode. Its power domain is 1.8 V, and the maximum clock frequency is 26 MHz. SPI is multiplexed from matrix keypad interface.

Table 27: Pin Description of SPI

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
KP_MKIN[1]	75	SPI1_CLK	DIO	SPI1 serial clock	1.8 V power domain. If unused, keep them open. When the module serves as master device, SPI1_CS and SPI1_CLK are in output state. When the module serves as slave device*, SPI1_CS and _SPI1_CLK are in input state.
KP_MKOUT[1]	74	SPI1_CS	DIO	SPI1 chip select	
KP_MKOUT[2]	76	SPI1_DOUT	DO	SPI1 data output	
KP_MKIN[2]	77	SPI1_DIN	DI	SPI1 data input	

The following figure shows a reference design of SPI connecting peripherals' circuit.

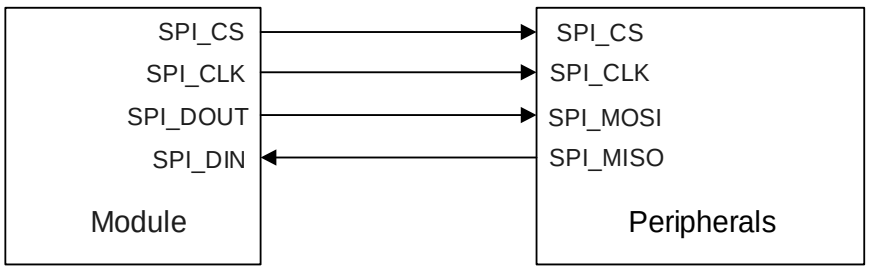


Figure 24: Reference Design of SPI (Module as Master)

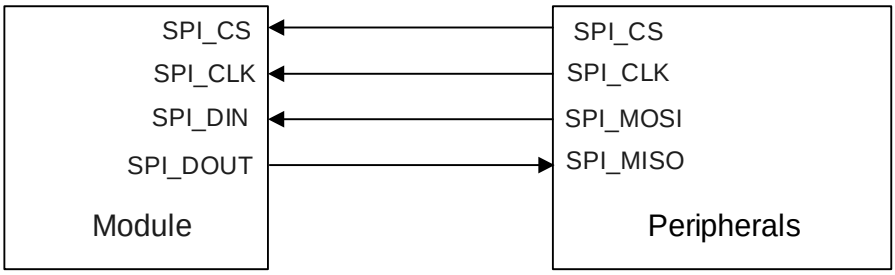


Figure 25: Reference Design of SPI (Module as Slave*)

NOTE

1. The module provides 1.8 V SPI. Use a voltage-level translator if your application is equipped with a 3.3 V system.
2. For more details about multiplexing, see ***document [8]***.

4.8. LCM Interface

The module's LCM interface supports display module with a maximum resolution of 240 × 320. It supports SPI four-wire single-line data transmission and RGB565 format output.

Table 28: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	1.8 V power domain. If unused, keep them open.
LCD_SPI_DOUT	50	DO	LCD SPI data output	
LCD_SPI_RS	51	DO	LCD SPI register select	
LCD_SPI_CS	52	DO	LCD SPI chip select	
LCD_SPI_CLK	53	DO	LCD SPI clock	
LCD_TE	78	DI	LCD tearing effect	

For reference design of LCM interface, see ***document [2]***.

4.9. Matrix Keypad Interface

The module supports 3 × 4 matrix keypad, see the following table:

Table 29: Pin Description of Matrix Keypad Interface

Pin Name	Pin No.	I/O	Description	Comment
KP_MKOUT[1]	74	DO	Matrix keypad output 1	1.8 V power domain. If unused, keep them open.
KP_MKIN[1]	75	DI	Matrix keypad input 1	
KP_MKOUT[2]	76	DO	Matrix keypad output 2	
KP_MKIN[2]	77	DI	Matrix keypad input 2	
USB_BOOT/ KP_MKOUT[4]	82	DO	Matrix keypad output 4	
KP_MKOUT[3]	86	DO	Matrix keypad output 3	
KP_MKIN[3]	87	DI	Matrix keypad input 3	

The reference design of matrix keypad interface, see ***document [2]***.

4.10. ADC Interfaces

The module supports two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 30: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep it open.
ADC1	96	AI		

You can use the following API to read the voltage value of ADC interfaces.

Table 31: Related API of ADC Interfaces

	QuecOpen	QuecPython
API	*ql_adc_read()*	*ADC.read()*

Table 32: Characteristics of ADC Interfaces

Category	Min.	Typ.	Max.	Unit
Input voltage at ADC0	0	-	1.2	V
Input voltage at ADC1	0	-	1.2	V
ADC resolution	-	-	12	bits

NOTE

1. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 respectively, and the required resistance of the two resistors that connected to power supply is between 100 kΩ and 1 MΩ.
2. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1 %. If the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5 % are recommended. See ***document [2]*** for details.
3. For more details about API of ADC interfaces:
   - QuecOpen: See ***document [6]***;
   - QuecPython: Please visit: https://python.quectel.com/doc/API_reference/zh/peripherals/misc.ADC.html.

4.11. Indication Signal

Table 33: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	

4.11.1. Indicate the module's network activity status

The module provides one network status indication pin NET_STATUS. It can drive corresponding LEDs.

Table 34: Module Network Status

Pin Name	Level Status	Module Network Status
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink slowly (1800 ms high/200 ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmission is ongoing

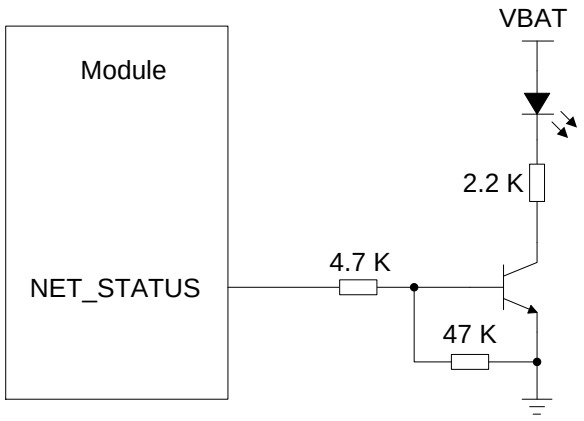


Figure 26: Reference Design of Network Status Indication

4.11.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on normally.

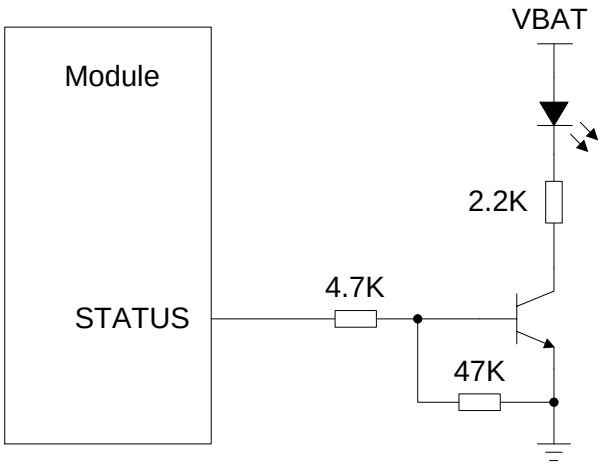


Figure 27: Reference Design of STATUS

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan* Antenna Interface

5.1.1. Antenna Interfaces & Frequency Bands

Table 35: Pin Description of LTE/Wi-Fi Scan Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	LTE/Wi-Fi Scan antenna interfaces	50 Ω characteristic impedance.

NOTE

The Wi-Fi Scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously.

Table 36: Operating Frequency of EC800K-CN/EG800K-CN

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025

LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

LTE-TDD B41 only supports 140 MHz (2535–2675 MHz).

Table 37: Operating Frequency of EG800K-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803

Table 38: Operating Frequency of EG800K-LA

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960

LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180

5.1.2. Transmitting Power

Table 39: RF Transmitting Power of EC800K-CN/EG800K-CN

Frequency Band	Max.	Min.
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 40: RF Transmitting Power of EG800K-EU

Frequency Band	Max.	Min.
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

Table 41: RF Transmitting Power of EG800K-LA

Frequency Band	Max.	Min.
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

5.1.3. Receiver Sensitivity

Table 42: Conducted RF Receiver Sensitivity of EC800K-CN/EG800K-CN (Unit: dBm)

Frequency Band	Receiver Sensitivity (Typ.)	3GPP Requirement
	Primary	
LTE-FDD B1 (10 MHz)	-99.0	-96.3
LTE-FDD B3 (10 MHz)	-99.0	-93.3
LTE-FDD B5 (10 MHz)	-99.5	-94.3
LTE-FDD B8 (10 MHz)	-98.5	-93.3

LTE-TDD B34 (10 MHz)	-100.0	-96.3
LTE-TDD B38 (10 MHz)	-99.5	-96.3
LTE-TDD B39 (10 MHz)	-100.0	-96.3
LTE-TDD B40 (10 MHz)	-100.0	-96.3
LTE-TDD B41 (10 MHz)	-99.0	-94.3

Table 43: Conducted RF Receiver Sensitivity of EG800K-EU (Unit: dBm)

Frequency Band	Receiver Sensitivity (Typ.)	3GPP Requirement
	Primary	
LTE-FDD B1 (10 MHz)	-98.5	-96.3
LTE-FDD B3 (10 MHz)	-99.0	-93.3
LTE-FDD B5 (10 MHz)	-99.0	-94.3
LTE-FDD B7 (10 MHz)	-97.0	-94.3
LTE-FDD B8 (10 MHz)	-99.0	-93.3
LTE-FDD B20 (10 MHz)	-99.0	-93.3
LTE-FDD B28 (10 MHz)	-98.5	-94.3

Table 44: Conducted RF Receiver Sensitivity of EG800K-LA (Unit: dBm)

Frequency Band	Receiver Sensitivity (Typ.)	3GPP Requirement
	Primary	
LTE-FDD B2 (10 MHz)	-98.5	-94.3
LTE-FDD B3 (10 MHz)	-98.5	-93.3
LTE-FDD B4 (10 MHz)	-98	-96.3
LTE-FDD B5 (10 MHz)	-98.5	-94.3
LTE-FDD B7 (10 MHz)	-96.5	-94.3
LTE-FDD B8 (10 MHz)	-99.0	-93.3

LTE-FDD B28 (10 MHz)	-98.5	-94.8
LTE-FDD B66 (10 MHz)	-98.5	-96.5

5.1.4. Reference Design

The reference design for antenna is as follows. Use a dual L-type matching circuit for the antenna interfaces for better RF performance. Capacitors C1 and C2 are not mounted by default.

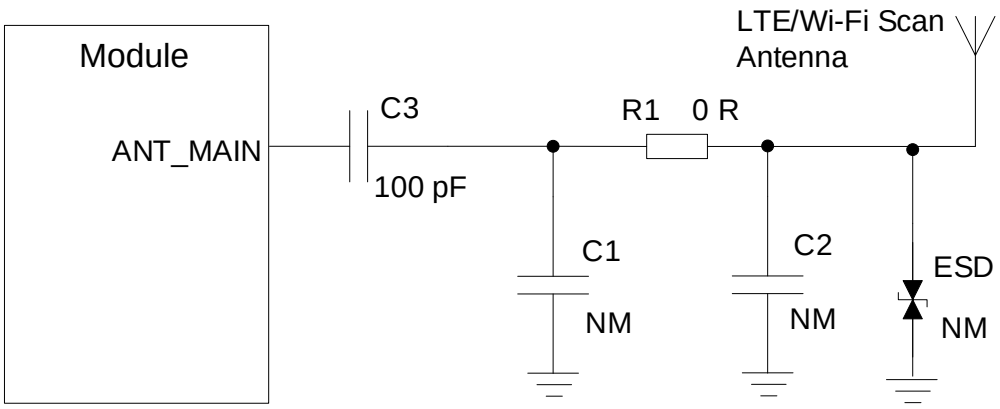


Figure 28: Reference Design of LTE/Wi-Fi Scan Antenna

NOTE

1. To reduce the coexistence problems and avoid the interference of receiving sensitivity, make sure that the isolation between antennas is more than 20 dB.
2. Place the dual L-type matching components (C3, R1, C1 and C2) to antennas as close as possible.
3. If there is DC power at the antenna ports, C3 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

5.2. GNSS

GNSS information of the module is as follows:

- The module supports GPS, BDS, GLONASS positioning system.
- The module supports NMEA 0183 protocol and does not output NMEA sentence by default. NMEA sentence can be output by USB interface or debug UART via API (update rate for positioning: 1 Hz).
- The module's GNSS function is disabled by default. It can be enabled via API.

Table 45: Related API of GNSS Usage

	QuecOpen	QuecPython
API	*ql_gnss_open()*	*quecgnss.gnssEnable*

NOTE

For more details about API of GNSS usage:

- QuecOpen: See ***document [1]***.
- QuecPython: Please visit: https://python.quectel.com/doc/API_reference/zh/gnsslib/quecgnss.html.

5.2.1. Antenna Interface & Frequency Bands

Table 46: Pin Description of GNSS Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	2	AI	GNSS antenna interface	50 Ω characteristic impedance. Only EG800K-CN supports GNSS function. For EC800K-CN, EG800K-EU and EG800K-LA, this pin is RESERVED. If unused, keep it open.

NOTE

Only EG800K-CN supports GNSS function.

Table 47: Operating Frequency

GNSS Constellation Type	Frequency Band	Unit
GPS	1575.42 ±1.023 (L1)	MHz
BDS	1561.098 ±2.046 (B1I)	
GLONASS	1597.5–1605.8 (L1)	

5.2.2. GNSS Performance

Table 48: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition		-159	
	Tracking		-160	
TTFF	Cold start @ open sky	Autonomous	28.11	s
		AGNSS start	5.96	
	Warm start @ open sky	Autonomous	27.37	
		AGNSS start	-	
	Hot start @ open sky	Autonomous	3.3	
		AGNSS start	-	
Accuracy	CEP-50	Autonomous @ open sky	2	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. Active antenna connection reference circuit is shown in the figure below.

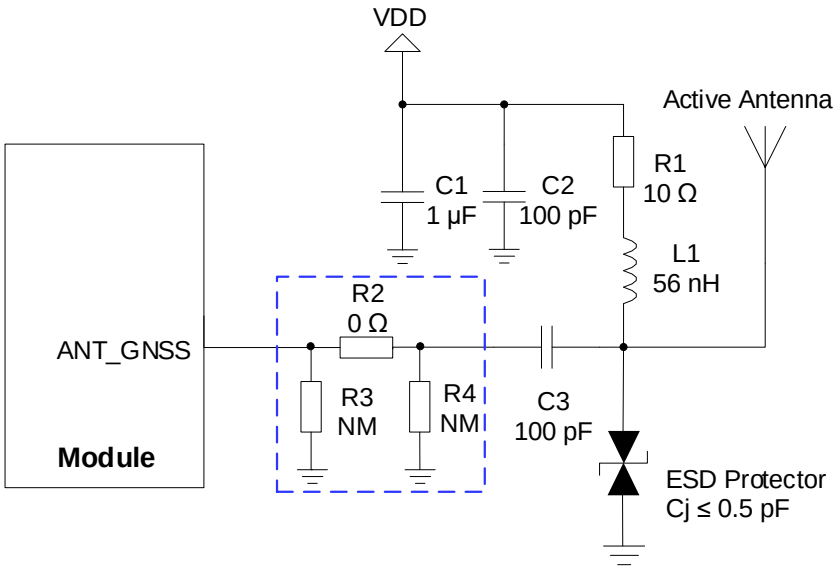


Figure 29: Reference Design of Active Antenna

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.2.3.2. Passive Antenna

Passive antenna connection reference circuit is shown in the figure below.

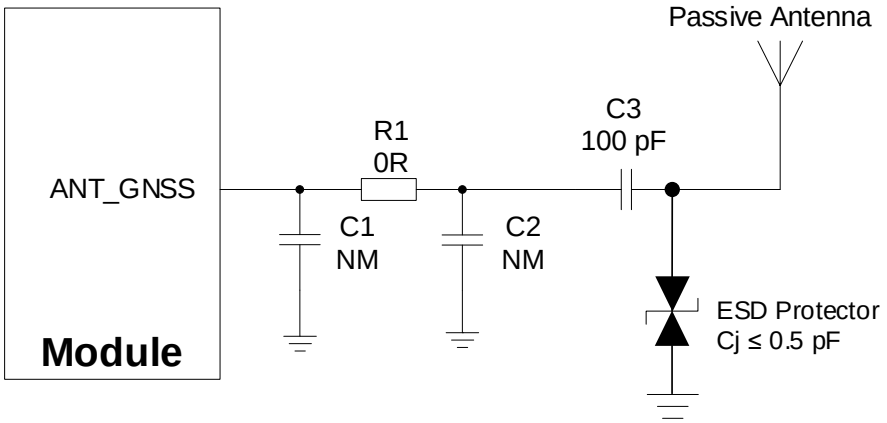


Figure 30: Reference Design of Passive Antenna

It is recommended to reserve a dual L-type matching circuit (C1, R1, C2 and C3) for better RF performance. Components (C1, R1, C2 and C3) of the dual L-type matching circuit shall be placed as close to the antenna as possible. C1, C2 are not mounted by default and a 0 Ω resistor is mounted on R1. Keep the characteristic impedance for RF trace as 50 Ω when routing and keep the trace as short as possible.

NOTE

1. The external LDO can be selected according to the active antenna requirements. If the module is designed with a passive antenna, then the VDD circuit is not needed.
2. It is recommended that the junction capacitance of the ESD protection component on the antenna interface not exceed 0.05 pF.
3. If there is DC power at the antenna ports, C3 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

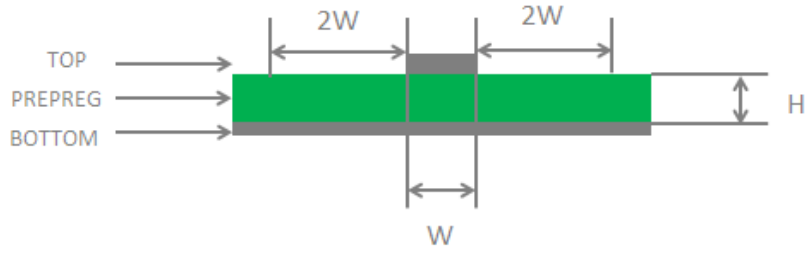


Figure 31: Microstrip Design on a 2-layer PCB

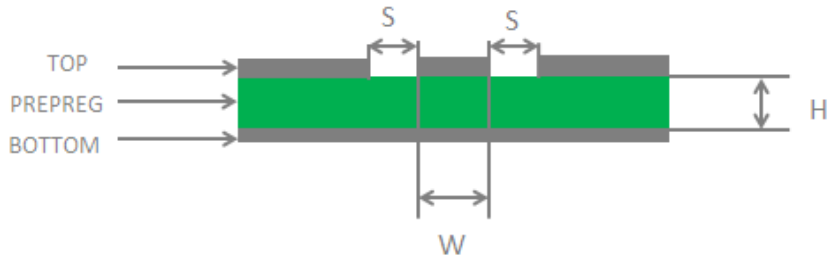


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

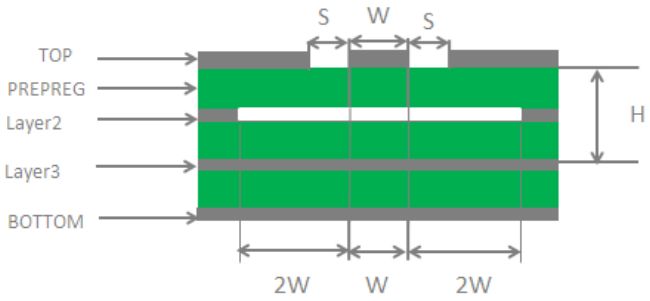


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

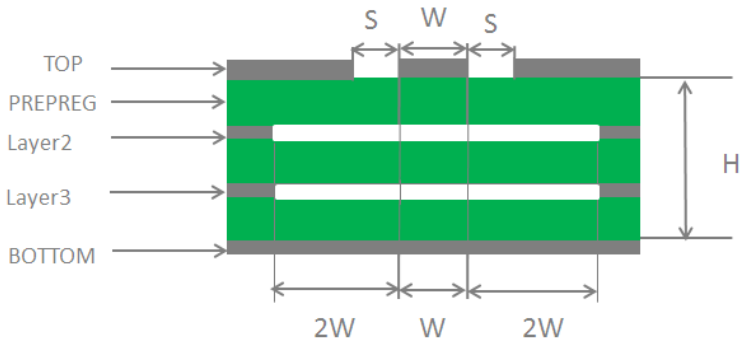


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [9]***.

5.4. Antenna Design Requirements

Table 49: Antenna Design Requirements

Antenna Type	Requirement
Cellular/Wi-Fi Scan	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
GNSS	● Frequency range: L1 (1559–1609 MHz) ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise coefficient: < 1.5 dB Active antenna embedded LNA gain: < 17 dB

5.5. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

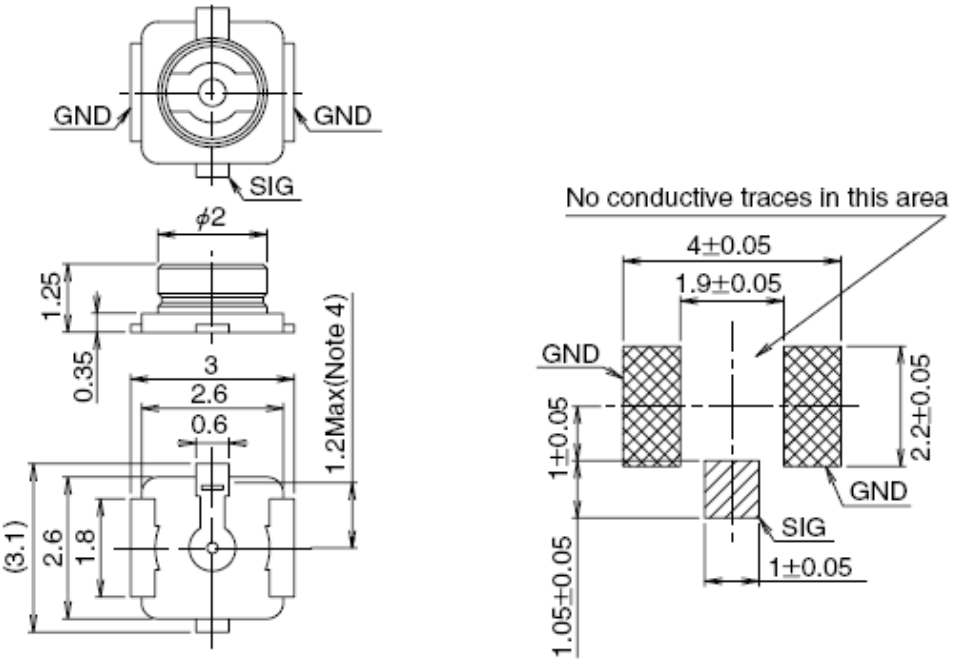


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

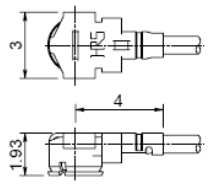
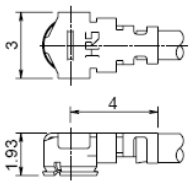
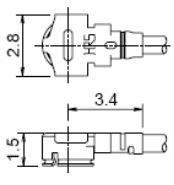
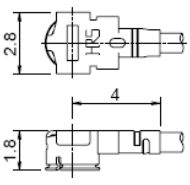
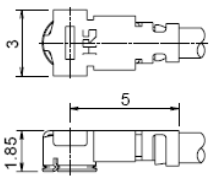
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

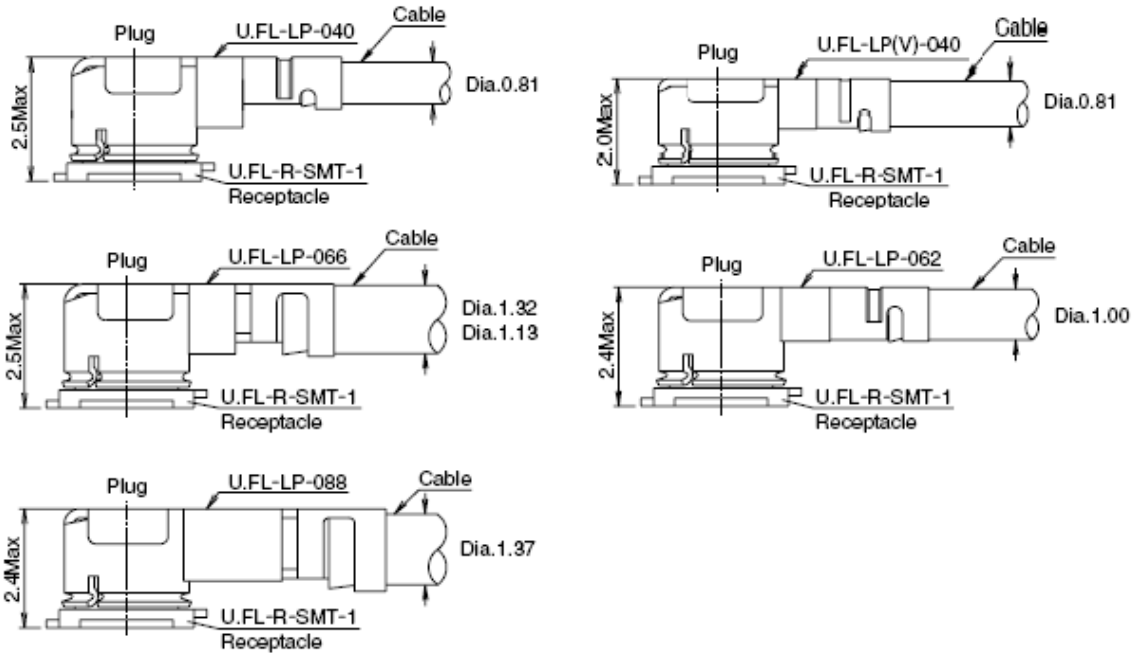


Figure 37: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 50: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	-0.3	6	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.2	V
Input voltage at ADC[0:1]	0	1.2	V
Peak current at VBAT	-	2	A

6.2. Power Supply Ratings

Table 51: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.3	V
I_{VBAT}	Peak supply current	At maximum power control level	-	-	1.5	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

6.3.1. Power Consumption of EC800K-CN

Table 52: Power Consumption of EC800K-CN

Mode	Condition	Typ.	Unit
Power Down Mode	Power off	6.42	μA
Sleep Mode	Minimum Functionality Mode (USB disconnected)	0.41	mA
	Airplane Mode (USB disconnected)	0.48	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.12	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.80	mA
	LTE-FDD @ PF = 64 (USB Suspended)	1.00	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.64	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.55	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.12	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.80	mA
	LTE-TDD @ PF = 64 (USB suspended)	1.00	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.64	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.56	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	7.98	mA
	LTE-FDD @ PF = 64 (USB connected)	20.69	mA
	LTE-TDD @ PF = 64 (USB disconnected)	8.00	mA
	LTE-TDD @ PF = 64 (USB connected)	20.69	mA
LTE data transmission	LTE-FDD B1	553	mA
	LTE-FDD B3	521	mA
	LTE-FDD B5	472	mA

	LTE-FDD B8	448	mA
	LTE-TDD B34	192	mA
	LTE-TDD B38	172	mA
	LTE-TDD B39	183	mA
	LTE-TDD B40	172	mA
	LTE-TDD B41	176	mA

6.3.2. Power Consumption of EG800K-CN

Table 53: Power Consumption of EG800K-CN

Mode	Condition	Typ.	Unit
Power Down Mode	Power off	6.15	μA
Sleep Mode	Minimum Functionality Mode (USB disconnected)	0.56	mA
	Airplane Mode (USB disconnected)	0.66	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.27	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.97	mA
	LTE-FDD @ PF = 64 (USB Suspended)	1.15	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.82	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.72	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.29	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.96	mA
	LTE-TDD @ PF = 64 (USB suspended)	1.14	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.81	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.73	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	7.96	mA
	LTE-FDD @ PF = 64 (USB connected)	19.46	mA

	LTE-TDD @ PF = 64 (USB disconnected)	7.98	mA
	LTE-TDD @ PF = 64 (USB connected)	19.46	mA
LTE data transmission	LTE-FDD B1	542	mA
	LTE-FDD B3	515	mA
	LTE-FDD B5	453	mA
	LTE-FDD B8	465	mA
	LTE-TDD B34	177	mA
	LTE-TDD B38	190	mA
	LTE-TDD B39	168	mA
	LTE-TDD B40	173	mA
	LTE-TDD B41	191	mA

6.3.3. Power Consumption of EG800K-EU

Table 54: Power Consumption of EG800K-EU

Mode	Condition	Typ.	Unit
Power Down Mode	Power off	7.47	μA
Sleep Mode	Minimum Functionality Mode (USB disconnected)	0.47	mA
	Airplane Mode (USB disconnected)	0.56	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.10	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.79	mA
	LTE-FDD @ PF = 64 (USB Suspended)	0.93	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.64	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.56	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	7.82	mA
	LTE-FDD @ PF = 64 (USB connected)	19.66	mA

LTE data transmission	LTE-FDD B1	543	mA
	LTE-FDD B3	483	mA
	LTE-FDD B5	531	mA
	LTE-FDD B7	600	mA
	LTE-FDD B8	509	mA
	LTE-FDD B20	482	mA
	LTE-FDD B28	510	mA

6.3.4. Power Consumption of EG800K-LA

Table 55: Power Consumption of EG800K-LA

Mode	Condition	Typ.	Unit
Power Down Mode	Power off	7.68	μA
Sleep Mode	Minimum Functionality Mode (USB disconnected)	0.46	mA
	Airplane Mode (USB disconnected)	0.69	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.2	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.88	mA
	LTE-FDD @ PF = 64 (USB Suspended)	1.06	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.73	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.64	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	7.43	mA
	LTE-FDD @ PF = 64 (USB connected)	19.0	mA
LTE data transmission	LTE-FDD B2	477.80	mA
	LTE-FDD B3	478.49	mA
	LTE-FDD B4	518.9	mA
	LTE-FDD B5	502.72	mA

	LTE-FDD B7	618.32	mA
	LTE-FDD B8	500.14	mA
	LTE-FDD B28	532.52	mA
	LTE-FDD B66	515.86	mA

6.4. Digital I/O Characteristics

Table 56: 1.8 V I/O Characteristics

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × VDDIO	VDDIO + 0.2	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDDIO	V
V_{OH}	High-level output voltage	VDDIO - 0.2	-	V
V_{OL}	Low-level output voltage	-	0.2	V

Table 57: USIM Low-voltage I/O Characteristics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	0	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD	V

Table 58: USIM High-voltage I/O Characteristics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	0	0.15 × USIM_VDD	V
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 59: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 60: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.	Unit
Normal Operating Temperature [11]	-35	+25	+75	°C
Extended Operating Temperature [12]	-40	-	+85	°C
Storage Temperature	-40	-	+90	°C

[11] Within this range, the module's indicators comply with 3GPP specification requirements.
[12] Within this range, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

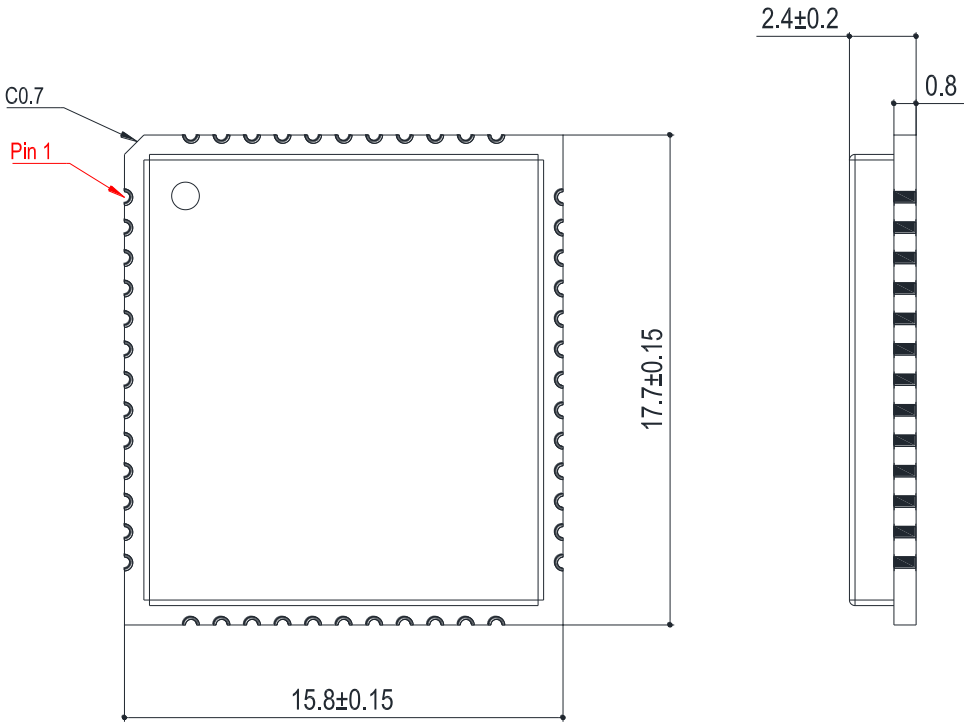


Figure 38: Top and Side Dimensions of EC800K-CN (Unit: mm)

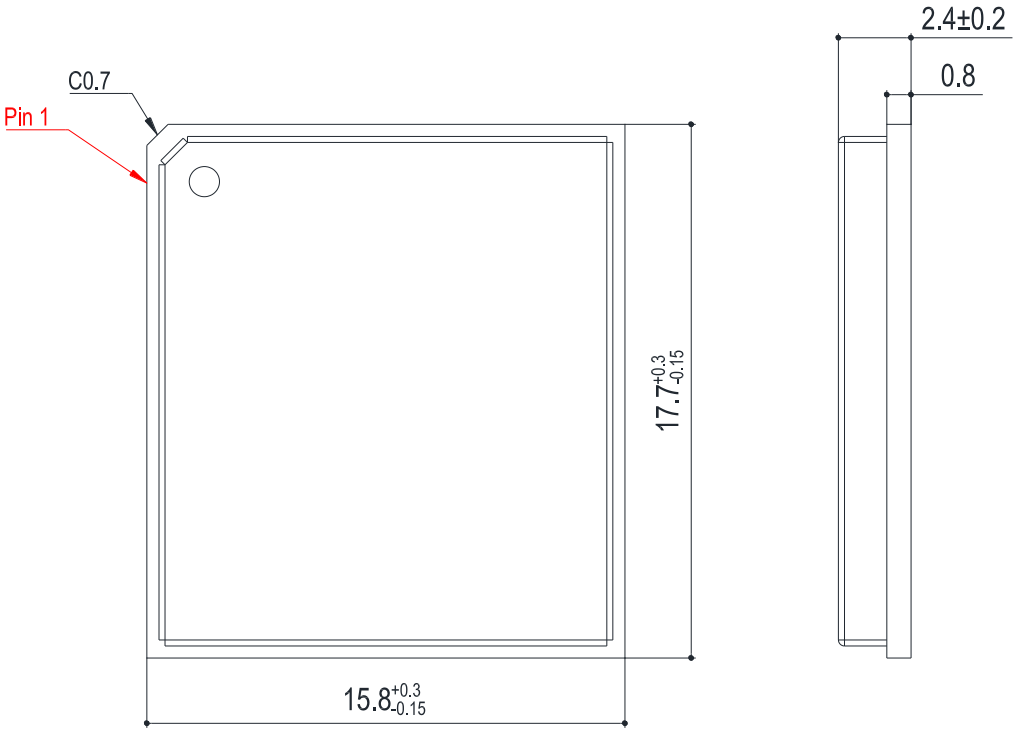


Figure 39: Top and Side Dimensions of EG800K Series (Unit: mm)

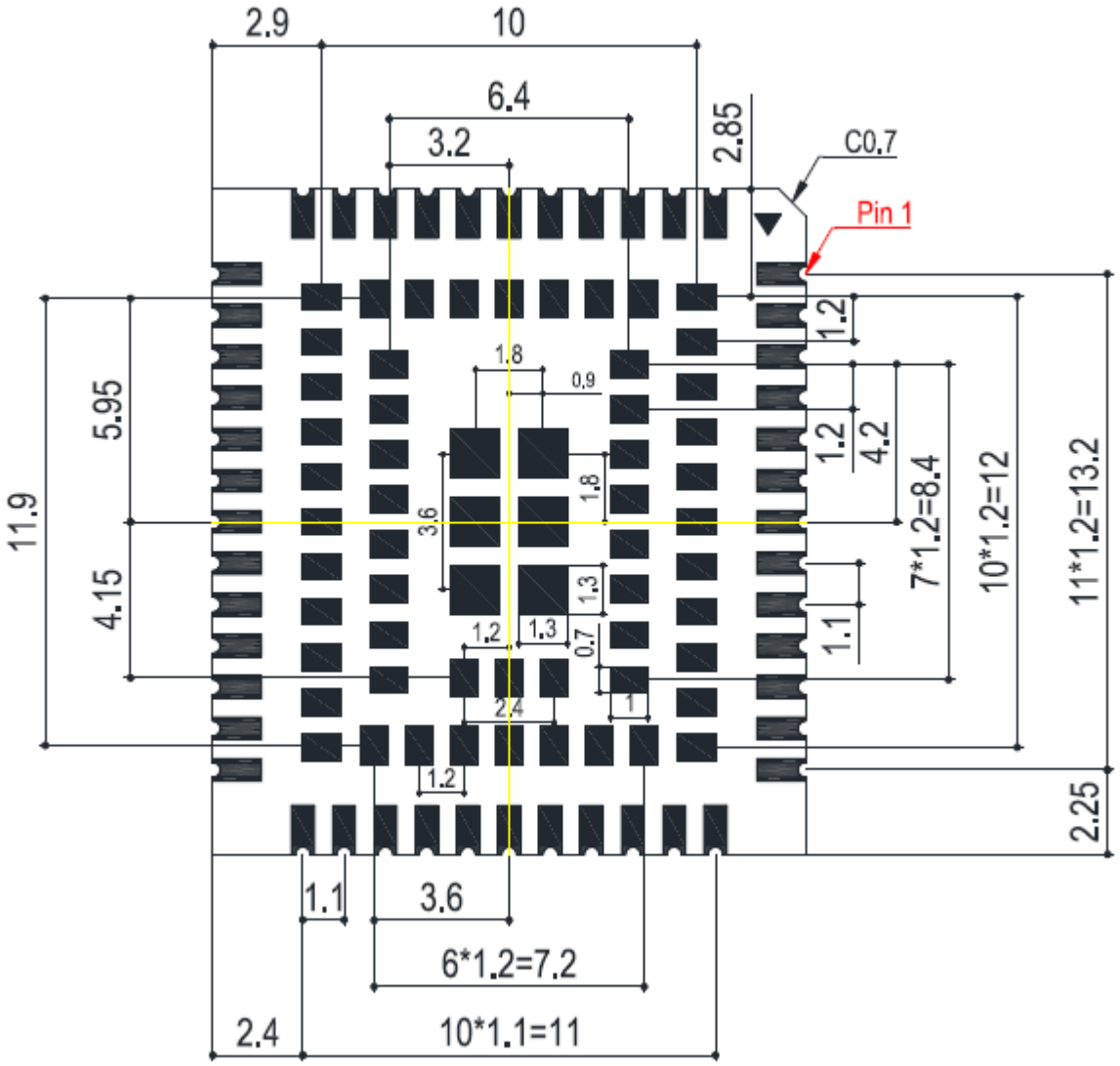


Figure 40: Bottom Dimension of EC800K-CN

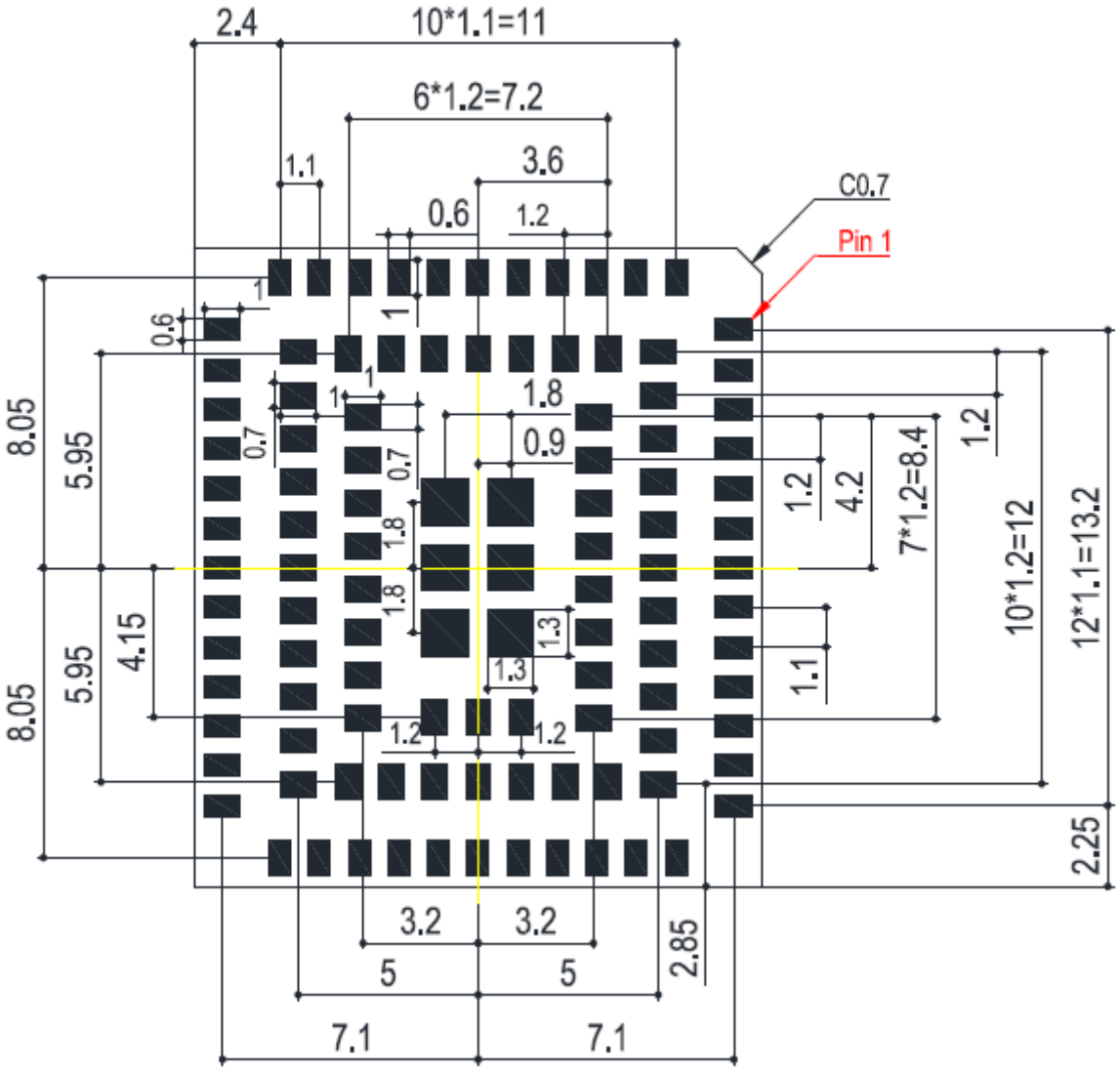


Figure 41: Bottom Dimension of EG800K Series

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

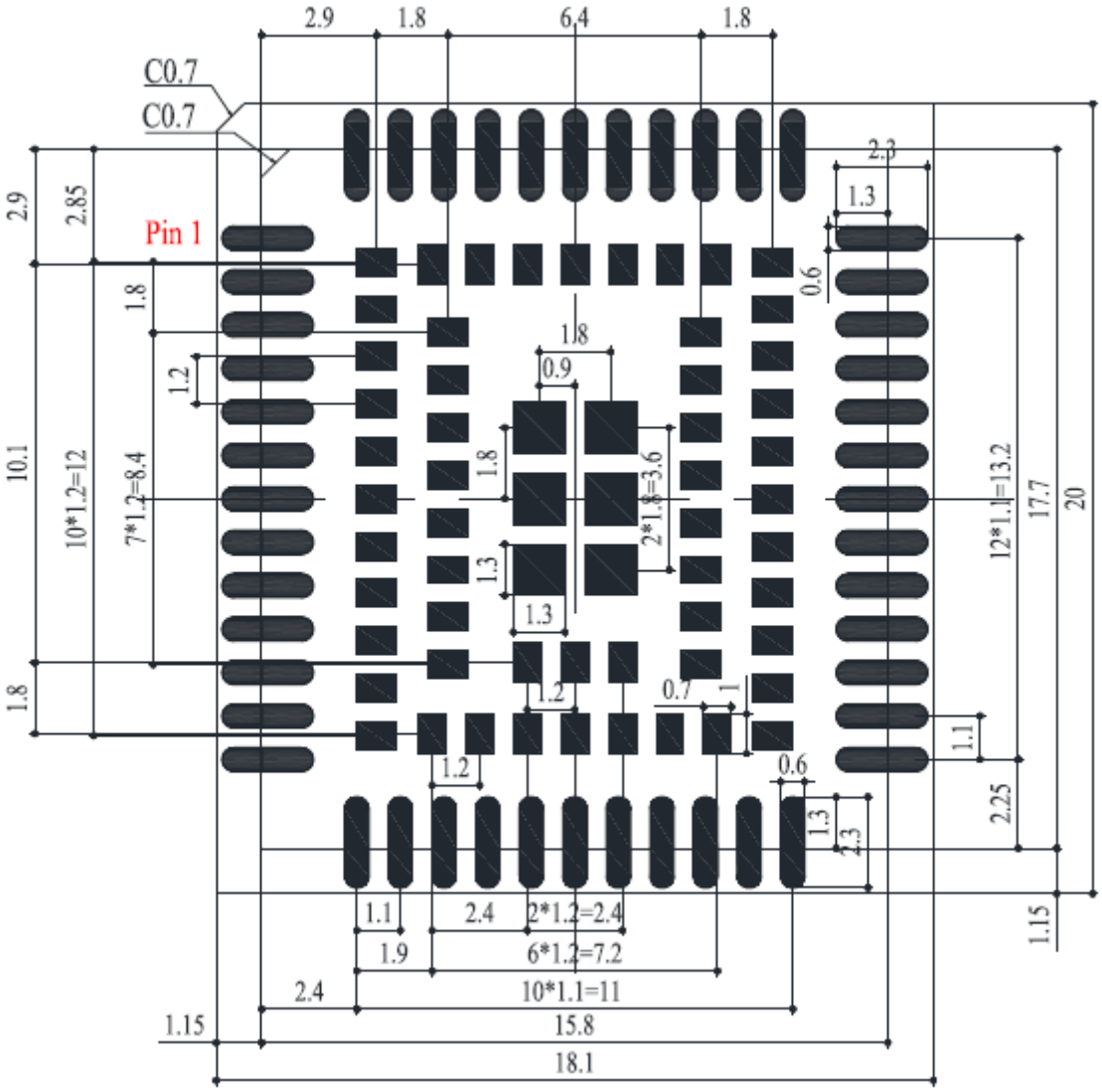


Figure 42: Recommended Footprint of EC800K-CN

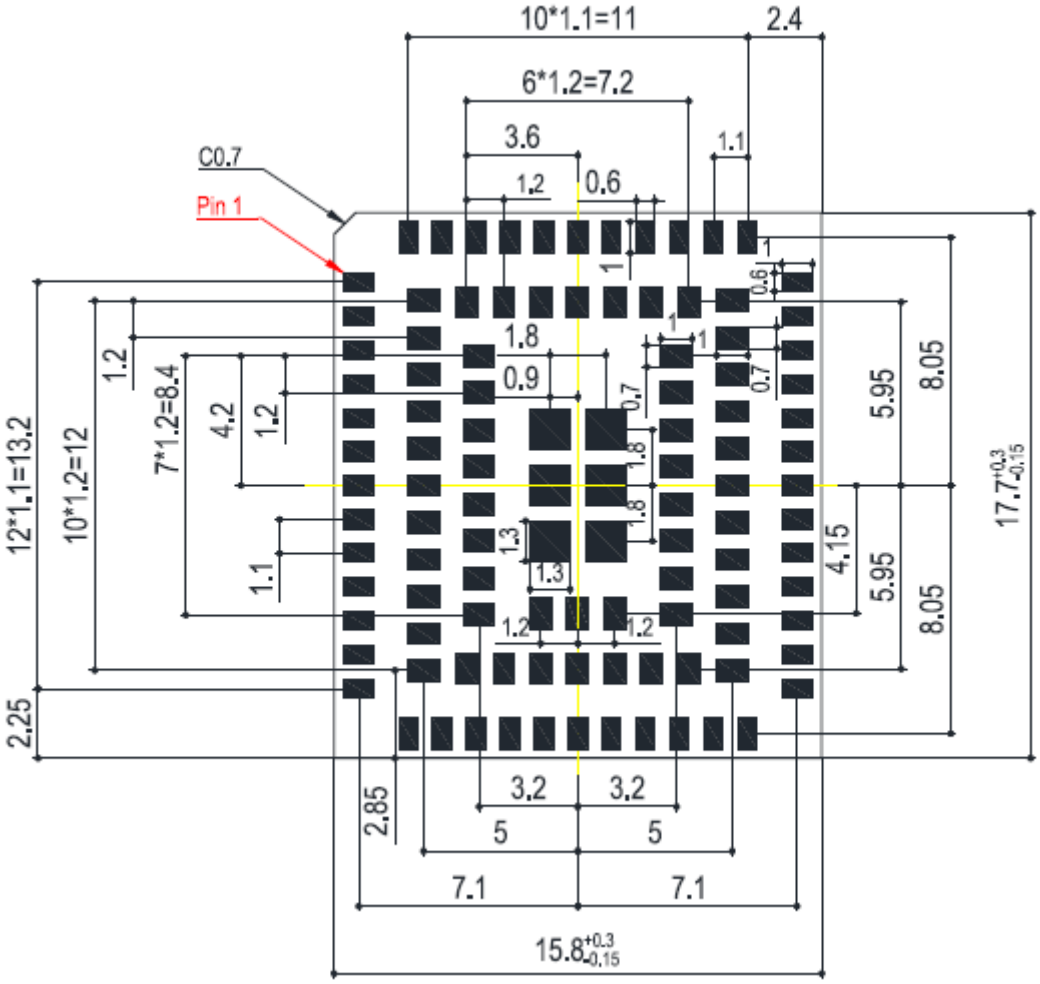


Figure 43: Recommended Footprint of EG800K Series

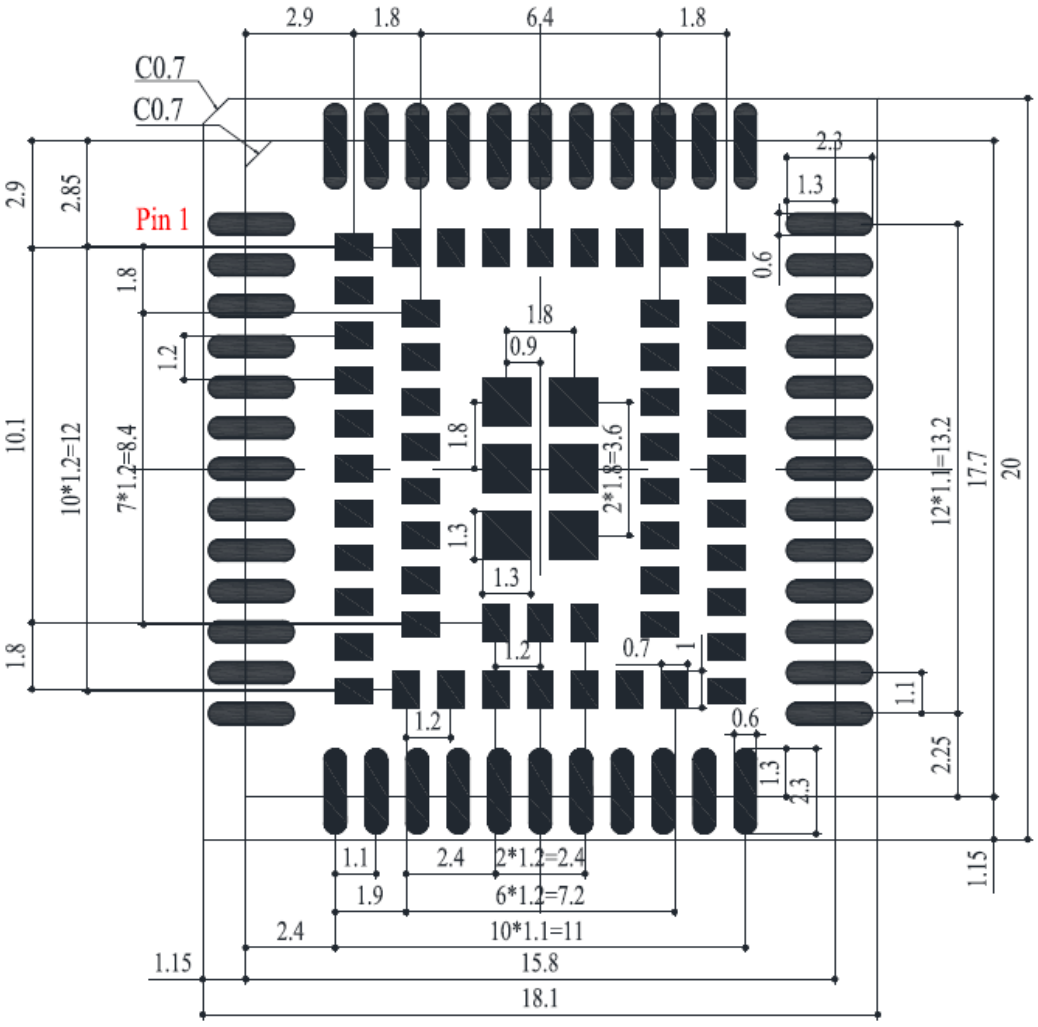


Figure 44: Recommended Compatible Footprint of EC800K & EG800K Series

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. If you consider the compatible design of EC800K and EG800K series modules, please refer to the compatible footprint & part. For the stencil design of the module, see the ***document [10]***.

7.3. Top and Bottom Views

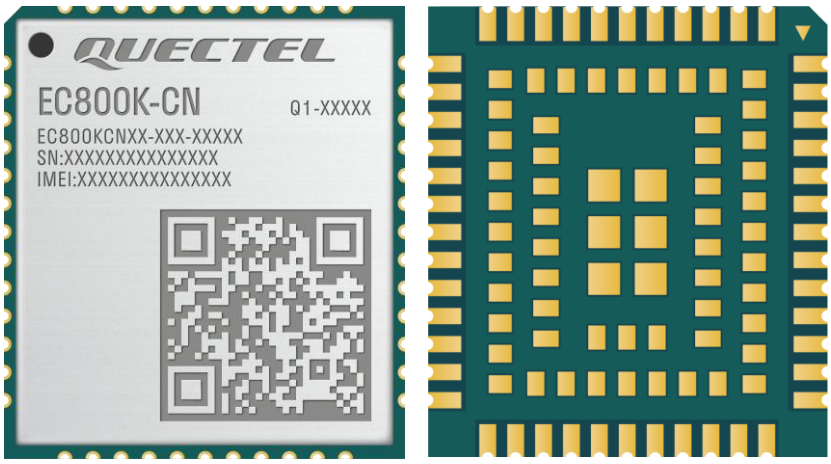


Figure 45: Top and Bottom Views of the EC800K-CN Module

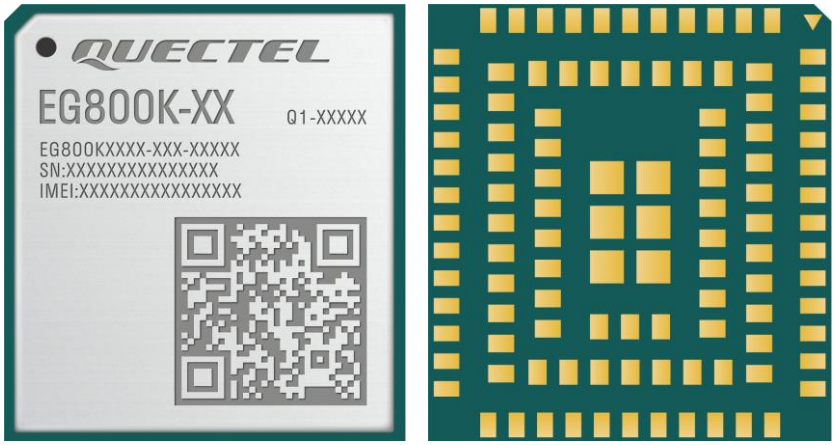


Figure 46: Top and Bottom Views of the EG800K Series Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [13] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[13] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for EC800K-CN is recommended to be 0.15–0.20 mm; the thickness of stencil for EG800K-CN, EG800K-EU and EG800K-LA is recommended to be 0.13–0.15 mm. For more details, see ***document [10]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

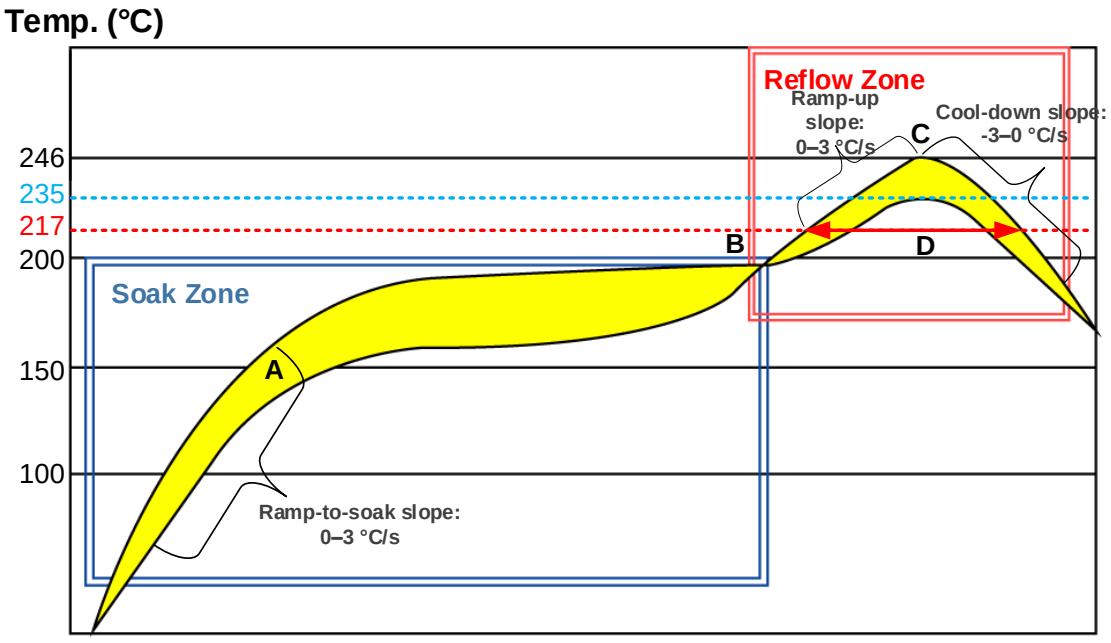


Figure 47: Recommended Reflow Soldering Thermal Profile

Table 61: Recommended Thermal Profile Parameters

Factor	Requirement
Soak Zone	
Ramp-up slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [11]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

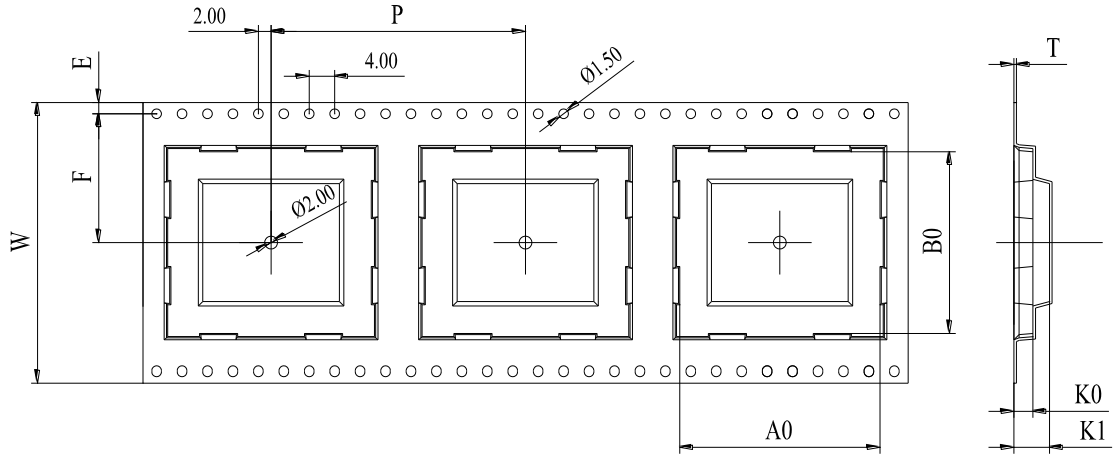


Figure 48: Carrier Tape Dimension Drawing (Unit: mm)

Table 62: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	4.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

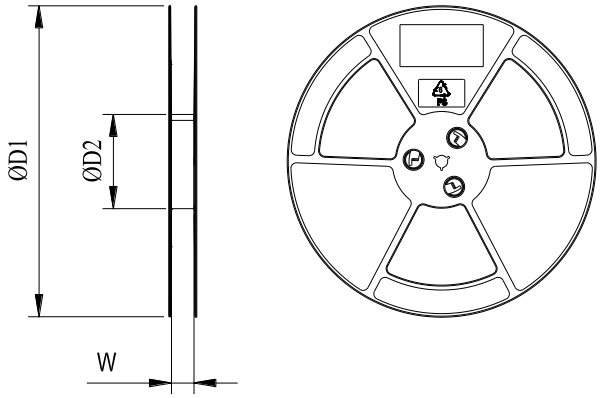


Figure 49: Plastic Reel Dimension Drawing

Table 63: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

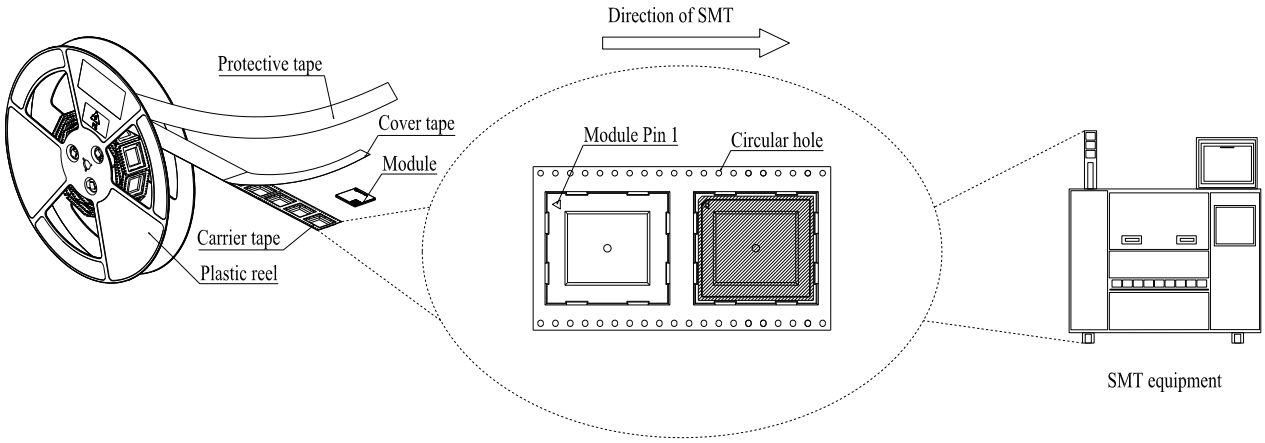
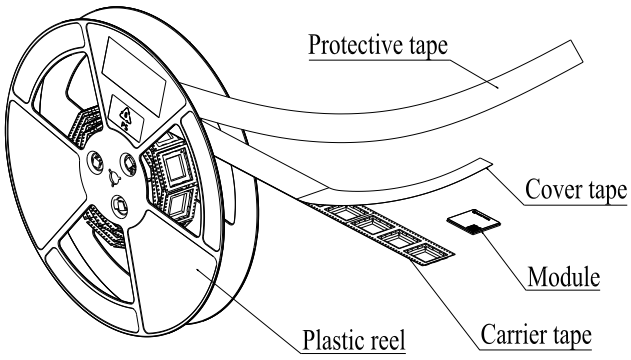


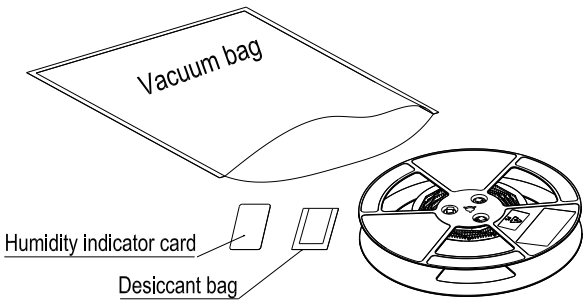
Figure 50: Mounting Direction

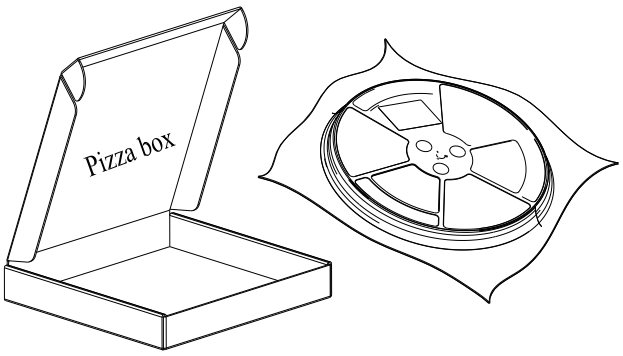
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

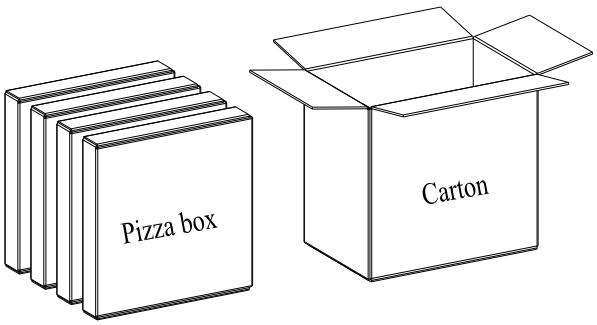


Figure 51: Packaging Process

9 Appendix References

Table 64: Related Documents

Document Name	
[1]	Quectel_ECx00x&EG800K&EG810M&EG915N&EG950A_Series_GNSS_Application_Guide
[2]	Quectel_EC800K&EG800K_Series_QuecOpen_Reference_Design
[3]	Quectel_LTE_OPEN_EVB_User_Guide
[4]	Quectel_ECx00x&EG800x&EG810M&EG91xN_Series_QuecOpen(SDK)_Device_Management_Guide
[5]	Quectel_ECx00x&EG800x&EG810M&EG91xN_Series_QuecOpen(SDK)_Lower_Power_Mode_Development_Guide
[6]	Quectel_ECx00x&EG800x&EG810M&EG91xN_Series_QuecOpen(SDK)_ADC_Development_Guide
[7]	Quectel_ECx00x&EG800x&EG810M&EG91xN_Series_QuecOpen(SDK)_Booting&Shutdown_Development_Guide
[8]	Quectel_EC800K&EG800K_Series_QuecOpen_GPIO_Configuration
[9]	Quectel_RF_Layout_Application_Note
[10]	Quectel_Module_Stencil_Design_Requirements
[11]	Quectel_Module_SMT_Application_Note

Table 65: Terms and Abbreviations

Terms	Description
3GPP	3rd Generation Partnership Project
API	Application Programming Interface
BDS	BeiDou Navigation Satellite System
bps	Bits per second

CEP	Circular Error Probable
CHAP	Challenge Handshake Authentication Protocol
Cj	Junction capacitance
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DFOTA	Delta Firmware Upgrade Over-The-Air
DRX	Discontinuous Reception
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GLONASS	Global Navigation Satellite System (Russia)
GND	Ground
GPS	Global Positioning System
GNSS	Global Navigation Satellite System
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMS	IP Multimedia Subsystem
$I_O$max	Maximum Output Load Current
Ipp	Peak Pulse Current
LCC	Leadless Chip Carrier (package)

LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone
NMEA	National Marine Electronics Association
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMS	Short Message Service
SPI	Serial Peripheral Interface

SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio